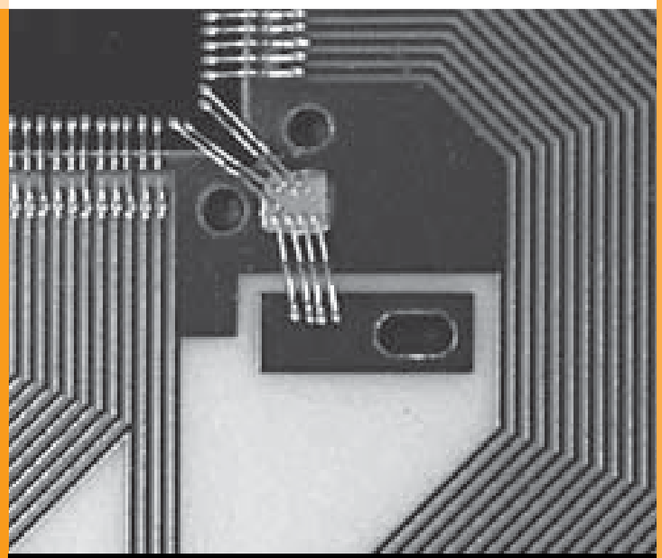
Thick Film
Thin Film
RF-PCB
Assembly/Packagng
Screening/Test

RHe
MICROSYSTEMS

Design Manual



RHe Design Manual

The following rules are effective for the draft of circuit boards and hybrid assemblies. The instructions are only valid for the layout design at RHe Microsystems GmbH. The rules are not intended to be exhaustive. All layouts should be designed in a close collaboration with RHe Microsystems GmbH.

Data file formats: GDS II, DXF, DWG, Extended GERBER (274-X) others on request

Compliance with mentioned values is depending on the properties of the used base material. A consultation is recommended.

Standard

These standard values can be used as a base for your layout and design process without request at RHe.

Special

These values are achievable by using special materials and/or special manufacturing equipment and methods. In any case a request for feasibility at RHe is recommended during early development/layout stage.

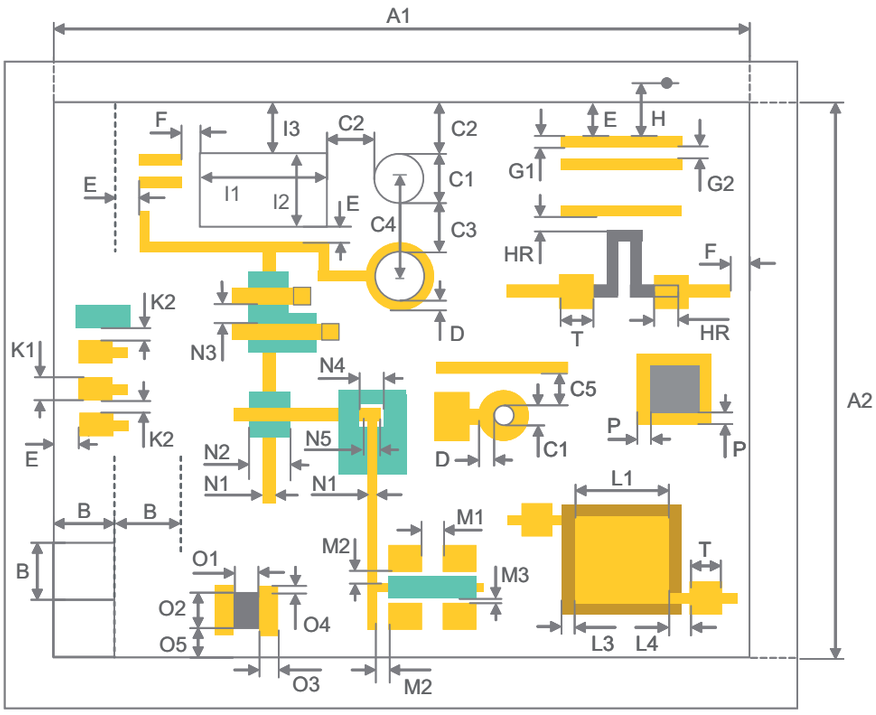
Special values should only be requested if a solution can't be found by using standard values.

Development

In this column named values are mostly custom made designs. As a developer/project leader please consider feasibility studies or separate sample manufacturing and use these parameters only in a tight collaboration with RHe in your products and constructions.

We look forward to be your partner for your special project. The manufacturing technologies will be especially designed to your requirements and series quantities.

Thick Film Drawing



Please note:

The drawing is a summary of all elements from thick film and thin film.

Because of this the selected design rule table below does not include all elements of the drawing.

Thick Film Design rules

		Standard	Special	Development
A1/A2	Tile dimension: 4“ x 4“, usable area:	≤ 95.6 x 95.6 mm²	x	x
A1/A2	Tile dimension: 6.5“ x 4.5“, usable area:	≤ 146.4 x 108.3 mm²	x	x
B	Dimension of single circuit boards on a tile:			
	Separation by laser scribing and breaking	≥ 3.0 x 3.0 mm²	≥ 2.0 x 1.5 mm²	
	Separation by sawing / dicing	≥ 2.0 x 2.0 mm²	≥ 1.5 x 0.6 mm²	
	Width of dicing channel (no metallisation in the channel allowed)	0.140 mm		
	Tolerances of single circuit board dimensions			
	Separation by sawing (after patterning)	± 0.050 mm	± 0.025 mm	± 0.015 mm
	Seperation by scribing and breaking (after patterning)			
	Substrate thickness: ≤ 0.381 mm	+ 0.100 / - 0.025 mm		
	Substrate thickness: ≤ 0.635 mm	+ 0.150 / - 0.050 mm		
	Substrate thickness: ≤ 1.270 mm	+ 0.200 / - 0.050 mm		
	Tolerance scribing line to scribing line	≤ ± 0.035 mm	≤ ± 0.020 mm	
C1	Drilled hole non-metallised: Ø */***	≥ 0.150 mm	≥ 0.100 mm	x
	Drilled hole for PTH: Ø (valid for 10-25 mil substrate thickness)*	0.150 mm	x	
	Tolerance drilled hole dimension	± 0.035 mm	± 0.025 mm	
C2	Distance hole circumference to substrate edge or cut-out	≥ Substrate thickness		
C3	Distance hole circumference to another hole circumference	≥ Substrate thickness	≥ 0.8 x Substrate thickness	
C4	Tolerance hole true center to another hole true center	≤ ± 0.050 mm	≤ ± 0.035 mm	
C5	Distance hole circumference to conductor 2nd layer on dielectric	≥ 0.200 mm	≥ 0.150 mm	x
D	Metallisation ring (rim) PTH around a drilled hole on top and bottom	≥ 0.250 mm	≥ 0.200 mm	
E	Distance conductor to substrate edge:			
	Separation by scribing and breaking	≥ 0.250 mm	≥ 0.200 mm	< 0.150 mm
	Separation by sawing/dicing	≥ 0.100 mm	≥ 0.050 mm	≥ 0.010 mm
	Distance conductor parallel to substrate or cut-out edge	≥ 0.200 mm		≥ 0.150 mm
F	Distance conductor orthogonal to substrate or cut-out edge	≥ 0.150 mm	≥ 0.100 mm	
	Conductor Line & Space:			
G1	Conductor width screen printed	≥ 0.200 mm	≥ 0.100 mm	≥ 0.080 mm
G2	Space between two conductors on ceramic	≥ 0.200 mm	≥ 0.150 mm	x
	Space between two conductors on dielectric	≥ 0.300 mm	≥ 0.150 mm	
G1	Conductor width, monolayer Au screen printed (etched)	≥ 0.150 mm	≥ 0.080 mm (≥ 0.040 mm)	
G2	Space between two conductors in Au screen printed (etched)	≥ 0.200 mm	≥ 0.080 mm (≥ 0.040 mm)	
I1/I2	Cut-outs (parallel to substrate edge)			
	Dimensions (measured at laser exit)*	≥ 1.000 mm x 1.000 mm	≥ 0.500 mm x 0.500 mm	x

		Standard	Special	Development
I3	Distance cut-out to substrate edge or another cut-out edge	≥ Substrate thicknss		
	Aligment tolerance cut-out to substrate edge cut or sawn	± 0.050 mm	± 0.020 mm	
	Aligment tolerance cut-out to substrate edge scribed/broken***	+ 0.250 / - 0.100 mm		
	Cavity (parallel to substrate edge)			
I1/I2	Dimensions (related to cavity base)	≥ 1.000 mm x 1.000 mm	≥ 0.500 mm x 0.500 mm	x
	Remaining substrate thickness in cavity/cavity base	≥ 0.130 mm	x (≥ 0.100 mm)	
I3	Distance cavity edge to substrate edge	≥ Substrate thickness		
	Tolerance cavity to substrate edge	≤ ± 0.250 ... ≥ ± 0.050 mm	± 0.030 mm	
K1	Wire bonding pad dimension: Standard	≥ 0.500 mm x 0.500 mm	≥ 0.300 mm x 0.300 mm	< 0.300 mm x 0.300 mm
K2	Wire bonding pad: Distance to other pads/solder stop/other...	≥ 0.200 mm	≥ 0.150 mm	x
M1 *****	Distance between solder pads	≥ 0.500 mm	≥ 0.250 mm	≤ 0.250 mm
M2 *****	Distance solder pads to conductor without covering	≥ 0.500 mm	≥ 0.300 mm	
M3 *****	Distance solder pad to overglaze/solder stop	≥ 0.150 mm	x	
	Conductor cross-over area			
N1	Conductor width underneath/on insulation of cross-over area	≥ 0.300 mm	≥ 0.200 mm	
N2	Insulation width and length	≥ 0.900 mm	≥ 0.700 mm	
N3	Distance conductor to conductor on insulation	≥ 0.300 mm	≥ 0.200 mm	
	Distance conductor to conductor at insulation edge	≥ 0.500 mm	≥ 0.400 mm	
N4	Via opening in insulation (sq or Ø)	≥ 0.6 x 0.6 mm²	≥ 0.4 x 0.4 mm²	
N5	Via pad dimension conductor/filling (sq or Ø)	≥ 0.4 x 0.4 mm²	≥ 0.35 x 0.35 mm²	
	Dimensioning of resistors (resistors parallel to substrate edge):			
O1	Resistor length	≥ 0.500 mm		
O2	Resistor width	≥ 0.700 mm		
O3	Overlapping zone resistor - conductor	≥ 0.350 mm	≥ 0.300 mm	≥ 0.250 mm
O4	Conductor margin at resistors	≥ 0.200 mm	≥ 0.150 mm	≥ 0.100 mm
O5	Distance resistor to substrate edge or scribe lines	≥ 0.500 mm	≥ 0.400 mm	
P	Pad for die attach			
	Metallisation ring circulating the die	0.150 mm		
T	Pad dimension for electrical measurements and laser trimming of resistors	≥ 0.500 mm x 0.500 mm	≥ 0.30 mm x 0.300 mm	< 0.300 mm x 0.300 mm
	x on request			
	* measured at laser exit, laser exit larger than entry, 7 ... 10 % of ceramic thickness larger on each edge			
	** depending on width and paste type			
	*** depending on substrate thickness			
	**** depending on substrate edge quality			
	***** Solder pads in high density packages need special dimensions – request in any case at RHe			

Thick Film materials

Substrate Material	Composition	Dielectric Constant [ε_r @ 25 °C]	Loss Tangent [tanδ @ 1 MHz]	Thermal Conductivity [W/mK @ 25 °C]	Coefficient of linear Thermal Expansion CTE [ppm/K]	Dielectric Strength [kV/mm]	Density [g/cm³]	Surface finish typical Ra [nm]	Thickness **								Processing				
									0.127 mm	0.178 mm	0.254 mm	0.381 mm	0.504 mm	0.635 mm	1.016 mm	1.270 mm	Laser drilling	Laser cutting	Cavity	Laser scribing	Sawing
Aluminium oxide ceramics 96 % (Al_2O_3)	as fired	9.5	0.001	26	6.4	> 19	3.75	< 900			x	x	x	x	x	x	x	x	x	x	x
Aluminum nitride ceramics (AlN)	as fired	9	0.001	180 – 190	4.7	> 20	3.30	≤ 600			x	x	x	x	x	x	x	x	x	x	x
Beryllium oxide ceramics (BeO 99.5 %)	as fired	6.8	0.0017	250	7.6	> 10	2.86	400													
Microwave-Ferrite																	x				x

** Thickness-Tolerance: Standard ± 10 %, other thickness in compliance with customer request
Other thicknesses available on request.

Conducturs:

Paste	Base Material	Fired Thick-ness in µm*	Rsq in mOhm/sq for mean fired thickness	Line & Space in µm	Processes/Applicable for			RoHS	Firing/Curing Temp. in °C
					Soldering	Die Attach	Wire Bonding		
AgPd	Al_2O_3	12 – 16	< 32	150	x			x	850
AgPd	AlN	13 – 15	< 25	150	x			x	850
AgPt	Al_2O_3	13 – 19	< 2.5	150	x			x	850
AgPt	AlN	9 – 11	< 65	150	x			x	850
Ag	Al_2O_3	14 – 18	1 – 2	150 - 200	x			x	850
Ag	AlN	9 – 11	< 3	125	x			x	850
Au	Al_2O_3	7 – 9	< 6.5	175		x	x	x	850
Au	AlN	8 – 12	< 6	100		x	(x) Au only	x	850
AuPt	Al_2O_3	13 – 17	60 – 100	150	x			x	850
Polymer Au	Al_2O_3	25 – 30	< 100	250				x	125

Resistors:

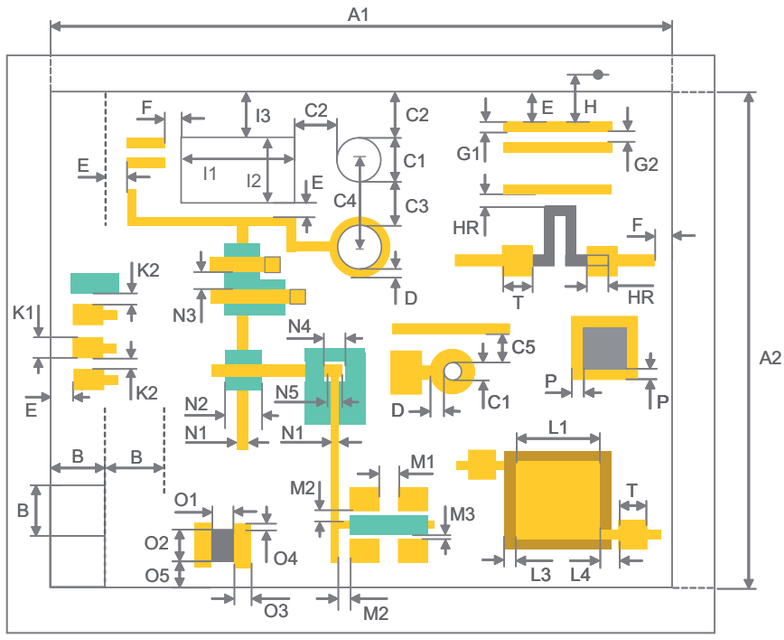
Paste	Base Material	Fired Thick-ness in µm*	Rsq in mOhm/sq	RoHS	HTCR in +/- ppm/K	Firing/Curing Temp. in °C	
Resistors	Al_2O_3	10 – 20	0.1 Ohm – 3 Ohm	x	25 – 75	850	
Resistors (decade system)	Al_2O_3	10 – 20	10 Ohm – 1 MOhm	x	50 – 125	850	
Resistors (decade system)	AlN	10 – 20	5 Ohm – 1 kOhm	x	100 – 150	850	

Insulation, Overglaze, Solder Stop:

Paste	Base Material	Fired Thick-ness in µm*	Via Resolution	Dielectric Constant	Loss Factor	RoHS	Firing/Curing Temp. in °C	
Dielectric	Al_2O_3	> 30	250 – 300	8 – 10 @ 1 MHz	0.5 %	x	850	
Dielectric	AlN	> 30	250 – 300	5 – 8 @ 1 MHz	0.2 %	x	850	
Overglaze	Al_2O_3	10 – 12				x	500	
Overglaze	AlN	14 – 16				x	650	
Polymer blue	Al_2O_3/AlN					x	150/200	
Polymer red	Al_2O_3/AlN					x	150	
Polymer Flex green	Al_2O_3/AlN					x	> 80	

* Fired thickness only reachable with multiple prints

Thin Film Drawing



Please note:

The drawing is a summary of all elements from thick film and thin film.

Because of this the selected design rule table below does not include all elements of the drawing.

Details for Resistors and Polyimid (Capacitors, Multilayer, Bridges etc.) please see separate table in chapter Thin Film metallisation.

Thin Film Design rules

		Standard	Special	Development
A1/A2	Tile dimension: 4“ x 4“, usable area:	88.0 x 90.0 mm²	92.0 x 92.0 mm²	x
A1/A2	Tile dimension: 2“ x 2“, usable area:	46.8 x 46.8 mm²	x	x
B	Dimension of single circuit boards on a tile:			
	Separation by laser scribing and breaking	≥ 3.0 x 3.0 mm²	≥ 2.0 x 1.5 mm²	
	Separation by sawing / dicing	≥ 2.0 x 2.0 mm ²	≥ 1.5 x 0.6 mm²	
	Width of dicing channel (no metallisation in the channel allowed)	0.140 mm		
	Tolerances of single circuit board dimensions			
	Separation by sawing (after patterning)	± 0.050 mm	± 0.025 mm	± 0.015 mm
	Separation by scribing and breaking (after patterning)			
	Substrate thickness: ≤ 0.381 mm	+ 0.100 / - 0.025 mm		
	Substrate thickness: ≤ 0.635 mm	+ 0.150 / - 0.050 mm		
	Substrate thickness: ≤ 1.270 mm	+ 0.200 / - 0.050 mm		
	Tolerance scribing line to scribing line	≤ ± 0.035 mm	≤ ± 0.020 mm	
C1	Drilled hole / PTH: Ø (measured at laser exit, laser entrance + 7 … 10%)	≥ 0.200 mm	≥ 0.150 mm	x

		Standard	Special	Development
C1	Min. ratio drilled hole to substrate thickness:	≥ 0.5	≥ 0.5	
	Tolerance drilled hole dimension	± 0.035 mm	± 0.025 mm	
C2	Distance hole circumference to substrate edge or cut-out	≥ Substrate thickness		
C3	Distance hole circumference to another hole circumference	≥ Substrate thickness	≥ 0.8 x Substrate thickness	
	Tolerance hole true center to another hole true center	≤ ± 0.020 mm		
	Tolerance hole true center to another hole true center, substrate stress annealed	≤ ± 0.035 mm		
D	Metallisation ring (rim) around a drilled hole on top and bottom	≥ 0.100 mm	≥ 0.070 mm	x (0 – 0.05 mm)
E	Distance conductor to substrate edge:			
	Separation by scribing and breaking	≥ 0.200 mm	≥ 0.100 mm	
	Separation by sawing / dicing	≥ 0.100 mm	≥ 0.050 mm	≥ 0.010 mm
	Distance conductor parallel to substrate edge or cut-out edge	≥ 0.200 mm		≥ 0.150 mm
F	Distance conductor orthogonal to substrate edge or cut-out edge	≥ 0.150 mm	≥ 0.100 mm	≥ 0.050 mm
G1/G2	Conductor Line & Space: *			
	Cu conductor width, Cu thickness 3 - 6 µm	0.050 mm	0.030 mm	0.020 mm
	Tolerance conductor width: Cu thickness up to 3 µm / 10 µm	± 0.005 mm / 0.007 mm	± 0.003 mm / 0.005 mm	
	Au conductor width, Au thickness up to 3 µm*	0.040 mm	0.025 mm	0.010 mm
	Tolerance conductor width: Au thickness up to 3 µm / 10 µm	± 0.003 mm / 0.005 mm	± 0.002 mm / 0.005 mm	± 0.002 mm / 0.004 mm
	Resistors and adhesive layer, with tolerance of ± 3 µm	0.040 mm	0.015 mm	
H	Alignment tolerance conductor to laser fiducial	± 0.030 mm	± 0.020 mm	
	Alignment tolerance top to bottom patterning	± 0.060 mm	± 0.030 mm	
HR	Alignment tolerance resistors to conductor	± 0.020 mm	± 0.050 mm	x
I1/I2	Cut-outs (parallel to substrate edge)			
	Dimensions (measured at laser exit, laser entrance + 7 … 10%)	≥ 1.000 mm x 1.000 mm	≥ 0.500 mm x 0.500 mm	x
I3	Distance cut-out to substrate edge or another cut-out edge	≥ Substrate thickness		
	Alignment tolerance cut-out to substrate edge cut or sawn	± 0.050 mm	± 0.020 mm	
	Alignment tolerance cut-out substrate edge scribed/broken**	+ 0.250 / - 0.100 mm		
I1/I2	Cavity (parallel to substrate edge)			
	Dimension (related to cavity base)	≥ 1.000 mm x 1.000 mm	≥ 0.500 mm x 0.500 mm	x
	Remaining substrate thickness in cavity / cavity base	≥ 0.130 mm	x (≥ 0.100 mm)	
I3	Distance cavity edge to substrate edge	≥ Substrate thickness		
	Tolerance cavity to substrate edge sawed	± 0.050 mm	± 0.020 mm	
K1	Wire bonding pad dimension: Standard	≥ 0.300 mm x 0.300 mm	x	
K1	Wire bonding pad: Parallel to wedge wire bonding direction	≥ 0.250 mm x 0.050 mm	x	
	Distance wire bonding pad to other pad types/solder stop	≥ 0.250 mm		
T	Pad dimension for electrical measurements and laser trimming of resistors	≥ 0.300 mm x 0.300 mm	≥ 0.250 mm x 0.250 mm	x
M1	Distance between two adjoining solder pads	≥ 0.500 mm	≥ 0.250 mm	
M2	Distance solder pads to conductor without covering	≥ 0.500 mm	≥ 0.300 mm	
	x on request			
	* depending on metallisation material, thickness, location and frequency of occurance of conductive tracks as well as surface quality of substrate			
	** depending on substrate thickness			

Thin Film metallisation

Metallisation Systems *							Processing				
Resistor	Adhesive layer	Barrier layer	Conductive layer	Barrier layer	Surface	Solder stop	Standard solder material 1)	Special solder material	Au wire bonding	Al wire bonding	Gluing
(TaN)***	TiW (50 nm)		Au (1.5 … 10 µm)**			Polymer, TiW		x	x		x
(TaN)***	TiW (50 nm)	Pd (250 nm)	Au (1.5 µm)			Polymer, TiW	x*		x		x
(TaN)***	TiW (50 nm)		Au (1.5 … 10 µm)**	Ni (1.5 … 5 µm)	Au (0.1 … 0.2 µm)	Polymer, TiW	x	x		x	x
(TaN)***	TiW (50 nm)		Au (1.5 … 10 µm)**	Ni (1.5 … 5 µm)	Au (0.9 … 1.2 µm)	Polymer, TiW	x	x	x		x
(TaN)***	TiW (50 nm)		Au (1.5 … 10 µm)**	NiP (2 … 5 µm)	Au (0.05 … 0.1 µm)	Polymer, TiW	x	x		x	x
	(TiW (50 nm))		Pt (25 nm … 800 nm)								x
(CrNi)***	TiW (50 nm)		Au (1.5 … 10 µm)**			Polymer, TiW		x	x		x
(CrNi)***	TiW (50 nm)	Pd (400 … 600 nm)	Au solder pads (0.05 … 0.1 µm) and Au wire bonding pads (5 µm) selective			Polymer, TiW	x*		x		x
(CrNi)***	CrNi (50 nm)		Cu (3 … 10 µm)	Ni (1.5 … 5 µm)	Au (0.1 … 0.2 µm)	Polymer	x			x	x
(CrNi)***	CrNi (50 nm)		Cu (3 … 10 µm)	Ni (1.5 … 5 µm)	Au (0.7 … 1.2 µm)	Polymer, NiO	x	x	x		x
(CrNi)***	CrNi (50 nm)		Cu (3 … 10 µm)	Ni (1.5 … 5 µm)	Au (1.2 … 1.8 µm)	Polymer, NiO		x	x		x
	CrNi (50 nm)		Cu (3 … 10 µm)	NiP (2 … 5 µm)	Au (0.05 … 0.1 µm)	Polymer	x	x		x	x

Metallisation Systems as multilayer *											
Resistor	Adhesive layer	1. Conductive layer	Isolation	2. Conductive layer	Barrier layer	Surface					
(TaN)***	TiW (50 nm)	Au (1.5 … 5 µm)**	Polyimid (3 … 5 µm)	TiW/Au (1.5 … 10 µm)**	Ni versions	Au version	x	x	x		x
	* Tolerance layer thickness: ± 20 %										
	** selective reinforcement of Au possible										
	*** if resistors required (in case of CrNi resistors adhesive layer n.a.), layer thickness depending on Rsq										
	x* containing Pb										
	1) Pb free, Ni ≥ 3 µm										

Resistors					
TaN	High stable	TCR: - 90 ppm / K ± 40 ppm / K			Tracking: < 5 ppm / K
CrNi	TCR adjustable	TCR adjustable between - 20 ppm / K and + 60 ppm / K			Tracking: < 5 ppm / K
Square resistance Rsq		20 Ω, 50 Ω, 100 Ω, tolerance: ± 15 %; 200 Ω, tolerance: ± 30 %			
Rectangular resistors:		R = RL* Rsq / RW			
Resistor geometry: Length > width		RL: ≥ 0.100 mm	RW: ≥ 0.050 mm		
Resistor geometry: Length < width		RL: ≥ 0.080 mm	RW: ≥ 0.150 mm		
Meander resistors:			RW: ≥ 0.050 mm	As „special“: min. RW: ≥ 0.030 mm	
Distance between adjoining resistors			≥ 0.050 mm		
Overlapping zone resistors with conductive tracks RÜ		Standard: ≥ 0.100 mm	Special: ≥ 0.050 mm	RG: Opposite resistors with shared overlapping zone	
Conductive track width at resistor overlapping zone RÜB		TaN-R: Double-side over RB each ≥ 0.020 mm; CrNi-R at Cu layer: 0 µm; CrNi-R at Au layer: 50 µm			
Laser trimming: Geometry / dimensions			RW: ≥ 0.100 mm	Resistance 75 – 80 % of final value	
Distance between resistors laser trimmed			≥ 0.150 mm		
Pad dimension for measurements and laser trimming		≥ 0.300 mm		As „Special“: min. ≥ 0.250 mm	
Tolerance after laser trimming		Standard: 1%	Special: ≥ 0.5 %	Development: ≥ 0.1 %, depending on resistor geometry	
Long-term stability at Rsq 20 Ω, 50 Ω, 100 Ω		≤ 0.5 %			
Heat dissipation / power loss		≤ 150 mW / mm² (at ~ 130°C, on Al_2O_3)		Depending on ceramic material, geometry and surrounding	
Temperature load		max. 150 °C, constant			

Polyimide on Au conductive layer				Calculation of capacitors	
	Layer thickness	3 … 5 µm		$C_{Polyimid} = \varepsilon_0 \cdot \varepsilon_r \cdot A / d$	d = layer thickness polyimide A = overlapping area L (Area capacity coating)
	Line width	≥ 0.050 mm		$\varepsilon_0 = 8.85 \cdot 10^{-12}$ [F / m]	
	Distance between polyimide patterning	≥ 0.050 mm		$\varepsilon_r = 3.2 \ldots 3.3$ (0 % … 50 % RH)	
	Vias in polyimide	≥ 0.100 mm x 0.100 mm / standard		≥ 0.050 mm x 0.050 mm / special	for multilayer
L1	Dimensions of capacitor plates on substrate and polyimide	minimal ≥ 0.050 mm x 0.050 mm			Used for: Solder stop, glue stop, conductive track cross over, multilayer, bridges, capacitors
L3	Overlapping of polyimide on capacitor plate	≥ 0.100 mm / standard		≥ 0.050 mm / special	
L4	Distance pads for capacity measurement to capacitor plate	≥ 0.100 mm / standard		≥ 0.050 mm / special	
T	Pad dimension for capacity measurement	≥ 0.400 mm x 0.400 mm		≥ 0.300 mm x 0.300 mm	
	Patterning mismatch upper capacity coating	± 0.020 mm			

Thin Film materials

Ceramic material	Composition	Dielectric Constant [ε_r @ 25 °C]	Loss Tangent [tan δ @ 1 MHz]	Thermal Conductivity [W / mK @ 25 °C]	Coefficient of linear Thermal Expansion CTE [ppm / K]	Dielectric Strength [kV / mm]	Density [g / cm³]	Surface finish typical Ra [nm]	Thickness **								Processing				
									0.127 mm	0.178 mm	0.254 mm	0.381 mm	0.504 mm	0.635 mm	1.016 mm	1.270 mm	Laser drilling	Laser cutting	Cavity	Laser scribing	Sawing/Dicing
Aluminium oxide ceramic 99,6 % (Al_2O_3)	as fired	9.9	0.0001	35	7	12	3.88	50 ... 100	x		x	x	x	x	x	x	x	x	x	x	x
Aluminium oxide ceramic 99,6 % (Al_2O_3)	polished	9.9	0.0001	35	7	12	3.88	5 .. 20	x		x	x	x	x	x	x	x	x	x	x	x
Aluminium oxide ceramic 99,6 % (Al_2O_3)	TPS polished	10.1	0.0001	35	6.3	12	3.95	≤ 26	x		x	x	x	x	x	x	x	x	x	x	x
Aluminium nitride ceramic (AIN)	as fired	8.9	0.001	170 – 190	4.6	20	3.30	≤ 600			x	x	x	x	x	x	x	x	x	x	x
Aluminium nitride ceramic (AIN)	lapped	8.9	0.001	170 – 190	4.6	20	3.30	≤ 600			x	x	x	x	x	x	x	x	x	x	x
Aluminium nitride ceramic (AIN)	polished	8.9	0.001	170 – 190	4.6	20	3.30	100			x	x	x	x	x	x	x	x	x	x	x
Calcium magnesium titanate ($CaMgTiO_3$)	polished	19.5	0.0002	4.2	8.6		3.80	13			x	x					x				x
Saphir	polished	10.0	0.0001	42	5	48	3.97										(x)	(x)			x
Quartz glass SiO_2 *	lapped	3.8	0.001	1.46	0.6	30	2.20	50 ... 1000		x	x						(x)	(x)			x
Quartz glass SiO_2 *	polished	3.8	0.000015	1.46	0.6	30	2.20	5 ... 20		x	x						(x)	(x)			x
Zircon substrate	as fired	11.0	0.0005	27	8		4.07	30 ... 130			x	x									x
Low alcali borosilicate glass / glass AF 45		6.2	0.0009	1	4.5	38	2.72			0.2	0.3	0.4	0.5	0.7				x			x
Dielectric materials and other ceramics ***		36 ... 100																			x
Microwave ferrite																	x				x

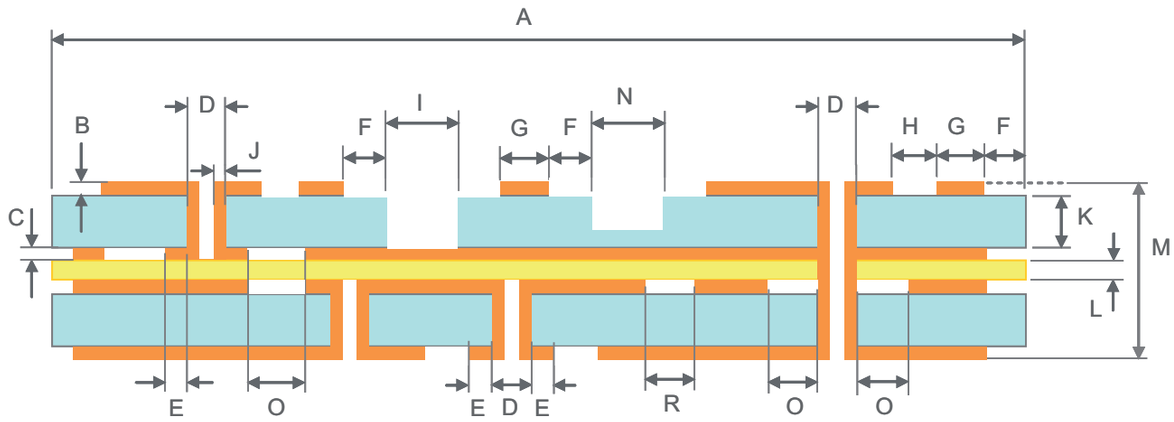
* Manufacturing only by order

** Thickness-Tolerance: Standard ± 10 %, premium ± 5 %; other thickness in compliance with customer request

*** Dielectric materials and other ceramics in compliance with customer request

(x) extern in Cicor Technologies Group

RF-PCB Drawing



RF-PCB Design rules

		Standard	Special	Development
A	Panel dimension for PCBs with PTHs and multilayer	275 x 195 mm²		
A	Panel dimension for PCBs without PTHs	370 x 220 mm²		
B	Cu tickness - base Cu outer layer	18 µm – 70 µm	9 µm – 70 µm	
B	Final Cu thickness - conductor outer layer	18 µm – 70 µm	9 µm – 70 µm	5 µm – 70 µm
C	Cu thickness - base Cu inner layer	18 µm – 35 µm		
C	Final Cu thickness - conductor inner layer	18 µm – 35 µm	18 µm – 50 µm	
D	Substrate hole (Via/PTH): Ø	≥ 0.500 mm	≥ 0.300 mm	≥ 0.200 mm
	Tolerance drilled holes to patterning	± 0.100 mm	± 0.075 mm	
	Tolerance drilled hole to drilled hole (depending on base material)	± 0.100 mm	± 0.050 mm	
E	Metallisation ring (rim) around via/PTH for top/bottom layer:			
	Subtractiv, for standard solder, Al wire bonding: Ø	≥ 0.200 mm	≥ 0.150 mm	
	Semiadditiv, for AuSn solder, Au wire bonding: Ø	≥ 0.120 mm	≥ 0.050 mm	
F	Distance conductor to outer edges/cut-outs / cavities	≥ 0.200 mm	≥ 0.050 mm	
G/H	Conductor Line & Space			
	for standard solder, Al wire bonding, final Cu thickness 18 µm	0.075 mm ± 0.020 mm		0.050 mm ± 0.010 mm
	for standard solder, Al wire bonding, final Cu thickness 35 µm	0.100 mm ± 0.030 mm		
	for AuSn solder, Au wire bonding, final Cu thickness 9 – 18 µm	0.075 mm ± 0.020 mm	0.075 mm ± 0.010 mm	0.050 mm ± 0.010 mm
	for AuSn solder, Au wire bonding, final Cu thickness 35 µm	0.100 mm ± 0.030 mm		
I	Cut-outs: Milling tool Ø	≥ 0.800 mm	≥ 0.200 mm	
	Radii in the corner of cut-outs	≥ 0.400 mm	≥ 0.100 mm	
	Tolerance cut-out/tolerance cut-out to patterning and via/PTH	± 0.100 mm	± 0.050 mm	
J	Cu thickness inside via/PTH	≥ 20 µm		

		Standard	Special	Development
K	Base material thickness	≥ 0.200 mm	≥ 0.100 mm	
L	Bonding film thickness	~ 0.038 mm		
L	Prepreg thickness	~ 0.100 mm		
M	Total thickness of multilayer (without surface)	≤ 3.200 mm	≤ 3.200 mm	
N	Cavities: Milling tools Ø	≥ 0.800 mm	≥ 0.200 mm	
	Tolerance of cavity depth	± 0.150 mm	± 0.100 mm	
	Radii in the corner of cavities	≥ 0.400 mm	≥ 0.100 mm	
	Tolerance cavity/tolerance cavity to patterning and via/PTH	± 0.100 mm	± 0.050 mm	
O	Distance PTH metallisation to inner conductor layer	≥ 0.500 mm		
R	Distance conductor to conductor inner layer	≥ 0.300 mm		

RF-PCB materials

Manufacturer	Material	Composition	Permittivity/ DC εr @ 10 GHz	Loss Tanget tan δ @ 10 GHz	Temperature coefficient W/mK	CTE ppm/K		
						x	y	z
Rogers	RO3003	PTFE/Ceramic	3.0	0.0013	0.5	17	17	24
Rogers	RO3203	Woven Glass	3.2	0.0016	0.5	13	13	58
Rogers	RO3210	Woven Glass	10.2	0.0027	0.81	13	13	34
Rogers	RO4003C	Hydrocarbon Ceramic	3.38	0.0027	0.64	11	14	46
Rogers	RO4350B	Hydrocarbon Ceramic	3.48	0.0037	0.62	14	16	50
Rogers	RT/duroid 5880	PTFE Glass Fiber	2.2	0.0009	0.2	31	48	237
Rogers	RT/duroid 6010LM	PTFE Ceramic	10.2	0.0023	0.78	24	24	24
Rogers	TMM 4	Hydrocarbon Ceramic	4.5	0.0020	0.7	14	14	20
Rogers	TMM 6	Hydrocarbon Ceramic	6.0	0.0023	0.72	16	16	20
Rogers	TMM 10	Hydrocarbon Ceramic	9.2	0.0023	0.76	16	16	20
Rogers	ULTRALAM 2000	PTFE Woven Glass	2.4 – 2.6	0.0019	0.24	15	15	200
Taconic	CER-10	PTFE-Woven fiberglass	10.0	0.0035	0.63	14	14	46
Taconic	RF-35	PTFE Glass Fiber	3.5	0.0018	0.24	19	24	64
Taconic	RF-60	PTFE-Woven fiberglass	6.15	0.0028	0.43	12	12	75
Taconic	TLC-32	PTFE Glass Fiber	3.2	0.0029	0.24	10	10	70
Arlon	AR1000	PTFE/Woven Fiberglass Ceramic Filled	10.0	0.0030	0.645	14	16	37
Isola	IS620	Glass Reinforced/ Modified Epoxy	5.5 – 3.7	0.0080	n/a	16	14	47
Dupont/Pyralux	AP8525	Polyimid	3.4	0.0030	n/a	25	25	25

Assembly/Packaging Design rules

Pos.	Reference	Standard	Special	Development
SMD Assembly				
	Pass. SMT components dimension min. for automatic assembly	0402	0201	01005
	Pass. SMT components dimension min. for manual assembly	0402	< 0 201	
	Board dimension max.	250 x 250 mm²		
	Placement accuracy	+/- 50 µm	+/- 30 µm	< +/- 30 µm
	Technological frame on tile for pick and place automat	10 mm	3 mm	
Lead-out, leaded or leadless				
	Contact pitch min.	0.8 mm	0.6 mm	
Die Attach wire bonded dies				
	Die dimension, edge length min.	0.5 mm	0.25 mm	0.1 mm
	Die dimension, edge length max.	30 mm	40 mm	80 mm
	Die thickness min.	0.3 mm	0.08 mm	< 0.08 mm
	Distance die to other glued components	≥ 0.2 mm	≥ 0.1 mm	≥ 0.05 mm
	Distance die to other soldered components (SMT)	≥ 1 mm	≥ 0.5 mm	
	Board dimension max.	150 x 150 mm²	250 x 250 mm²	
	Placement accuracy	+/- 30 µm	+/- 20 µm	<+/- 20 µm
Die Attach flip chip				
	Die dimension, edge length min.	0.5 mm	0.25 mm	0.15 mm
	Die dimension, edge length max.	5 mm	10 mm	> 10 mm
	Bump pitch min.	250 µm	150 µm	100 µm
	Bump quantity	≤ 100	≤ 400	> 400
Wire Bonding, ultrasonic, thermosonic, wedge-wedge, ball-wedge				
	Wire diameter Au min.	25 µm	17 µm	
	Wire diameter Au max.	38 µm	75 µm	
	Wire diameter Al min.	25 µm		
	Wire diameter Al max.	300 µm	500 µm	
	Wire diameter Pt		12.5 µm	
	Die bond pad min.	80 x 80 µm²	50 x 50 µm²	< 50 x 50 µm²
	Wire pitch	100 µm	50 µm	< 40 µm
	Bonding bridge length min. (in one height level)	500 µm	300 µm	< 300 µm
	Bonding bridge length max. in one height level, depending on wire diameter)	5 mm	10 mm	> 10 mm
Ribbon Bonding, thermosonic				
	Ribbon Au diameter	60 x 20 µm² 120 x 20 µm² 300 x 12.5 µm²		
Parallel Seam Sealing				
	Package dimension min.	3 x 3 x 3 mm³		
	Package dimension max.	135 x 50 x 30 mm³		
	Fine leak test volume max.	16 cm³		
Beam Lead Bonding		available		
Gap Welding		available		

Assembly/Packaging materials

Adhesives/coating materials					
Manufacturer	**Reference**	**Properties**	**Thermal Cond.**	**CTE**	**Operating Temp.**
			W/mK	**ppm/K**	**°C**
Epo-Tek/Polytec	H2OE	electrical conductive	2.9	31	- 55 / + 200
Epo-Tek/Polytec	H2OE-PFC	electrical conductive	3.2	21	- 55 / + 200
Epo-Tek/Polytec	H31D	electrical conductive	3.5	42	- 55 / + 200
Epo-Tek/Polytec	H37MP	electrical conductive	1.6	40	- 55 / + 200
Epo-Tek/Polytec	H72	thermal conductive	0.6	29	- 55 / + 250
Epo-Tek/Polytec	353ND	optic	N. A.	54	- 55 / + 250
Tracon	Ablebond 8-2	thermal conductive	1.5	40	- 55 / + 150
Panacol-Elosol	Elecolit 601	thermal conductive	1.1	35	- 60 / + 175
Ablestik	Ablefilm 5020 K	thermal conductive	0.7	45	
Emerson & Cuming	AMICON 50300	Glob top PCB	0.6	18	- 55 / + 125
Emerson & Cuming	AMICON 50302	Glob top ceramics	0.5	30	- 55 / + 125
Loctite	Hysol FP4460	Glob top ceramics		20	- 65 / + 125
Loctite	Hysol FP4650	Glob top ceramics		15	- 65 / + 125

Bonding wires					
Wire material	**Diameter µm**	**Elongation %**	**Hardness**	**Breaking load cN**	
Al	300	8 – 12		600 – 800	
AlSi1%	25	> 1		11 – 14	
AlSi1%	30	> 1		16 – 21	
Au	17.5	2 – 5	HD6	> 5	
Au	17.5	4 – 8	HD2	>1.5	
Au	25	4 – 7	HD1	> 7	
Au	25	2 – 6	HD5	> 9	
Au	30	2 – 6	HD2	12 – 16	

Solder material				
Material	**Melding point °C**			
	Liquidus	**Solidus**		
SnIn52	125	118		
SnBi58	138	138		
InPb30	175	165		
Sn62Pb36Ag2	179	179		
SnPb40	191	183		
SnAg3.5Cu0.7	220	217		
SnAg3.5	221	221		
AuSn20	280	280		

Assembly/Packaging Heat sink materials

Material	Density	CTE	Thermal Cond.
	g/cm³	ppm/K	W/mK
W(20)Cu	14.3	6.4	180
Mo(30)Cu	9.7	7.5	183
Cu	8.9	17	400
Kovar	8.1	5.9	17.5
Stahl	7.8	12.5	50
AlSi7Mg	3	6 – 7	180 – 210
Hivol (AlSi)	3	6.8	226
AlSiC	3	6.7	180 – 210
Al_2O_3	3.9	7	25
AlN	3.2	4.5	180
Al	2.7	23.4	220
Si	2.3	4.7	148
GaAs	5.3	5.4	46
Al Graphite	2.3	8.2 – 8.4	140 – 205

MAC (Micro Assembly Center) Services

Assembly from different boards, substrates and PCB‘s

Due to the expansion of the micro assembly technology RHe can now offer a wide range of assembly services in combination with the whole product portfolio:

- Thin film substrates (in-house manufacturing) for microwave applications, opto-electronic components and thermal management
- Thick film substrates (in-house manufacturing) microwave and power modules
- Special RF- and Microwave PCB’s
- Standard FR4, rigid, rigid-flex and flex boards as well as multilayer
- Combination of different boards and materials in one module
- Assembly of board on base plates, on heatsinks and in housings

Board assembly

- Different parts and components: standard SMT (0201), THT, µBGA/BGA, QFP, CSP, components for microwave applications, RF connectors, LED’s, photodiodes, laser diodes, crystals, active and passive optical components
- Automatic and manual Die-Attach: COB for Bare Dies/ASIC’s, wire bonding, Flip-Chip, MIC/MMIC’s processing from wafer or waffle pack
- Solder processes: with flux, with Pb, RoHS compliant, special solder; fluxless soldering in vacuum optional with positioning control and with formic acid, inert gas, hydrogen; rework services for soldered SMT components like BGA or QFP
- Gluing processes: high accuracy automatically dispense, stamp print; thermal/electrical glue or adhesive foil

Hybrid- and Module Assembly

- Automatic assembly of parts and components with a high precision microassembly system and with an integrated solderstation
- Plasma cleaning for parts, components and boards
- Fully automatic die bonding, flip chip bonding and assembly with components (e. g. MCM)
- Assembly of ceramic substrates, PCB’s or power components on base plates, in housings with soldering or epoxy (conductive/non-conductive)
- Assembly of substrates and boards on heatsinks and sandwich heatsinks
- Automatic and manual wire bonding: Ball-Wedge, Wedge-Wedge; ultrasonic, thermosonic, Au-/Al-/AlSi-Pt-wire, thin wire, heavy wire; ribbon bonding
- Beam lead bonding
- Gap welding
- Connecting with standard leadframes (SIL/DIL) customized leadframes, special solutions
- Different types of RF connectors

Circuit module protection

RHe offers the following sealing processes for hybrids or electronic assemblies (hermetic/quasi-hermetic):

- Glob top
- Conformal coating
- Assembly of parts, modules and subassemblies in standard housings/customised housings
- Hermetic sealing or soldering (option: filled vias)
- Gluing or soldering of metal or ceramic frames on boards/substrates
- Gluing or soldering of lids on frames
- Frames with metal or glass lids (glued/soldered)

Capabilities Screening/Test

Procedure	Range min	Range max
Burn-in	- 20 °C	+125 °C
Temperature / humidity storage	- 60 °C 15 % relative humidity	+150 °C 95 % relative humidity
Thermal cycling	- 60 °C	+150 °C
Acceleration	Zentrifuge, Biofuge Primo	
Leak test	Device for Gross and Fineleak test	Fineleak test: 10^{-8} mbar x l x s^{-1}
Operating live test	- 20 °C	+125 °C
Testing of the generic parameters U - Voltage I - Current R - Resistor C - Capacity F - Frequency	Standard measurement devices RF-functional test DC-functional test	up to 50 GHz
Mechanical shock, vibration	external	
PIND (particle impact noise detection)	external	

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