MCR100

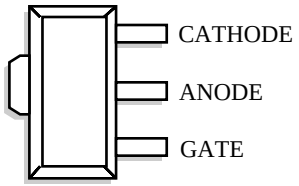
Sensitive Gate Silicon Controlled Rectifiers
Reverse Blocking Thyristors

Features:

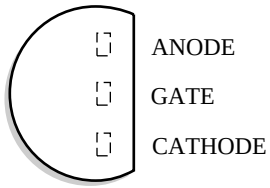
- Driven directly with IC and MOS device.
- Feature proprietary, void-free glass passivate chips.
- Available in voltage ratings from 200 to 600 volts. (VDRM and VRRM)
- Sensitive gate trigger current.
- Designed for high volume, line-powered control application in relay lamp drivers for large thyristors.

Pin Configuration – TOP VIEW

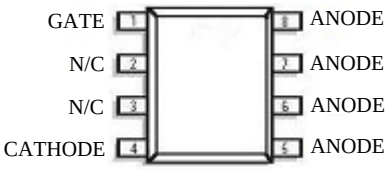
SOT-89 (S)



TO-92 (LP)



SOIC (D)



Ordering Information

MCR100 X X X

Circuit Type:
Silicon Controlled Rectifiers

Voltage Range:
4U = 200V
6U = 400V
8U = 600V

Package Option:
B = Bulk
T = Tube
A = Ammo
N = Tape and Reel (13” Reel Dia)

Package Style:
S = SOT-89
D = SOIC
LP = TO-92

Absolute Maximum Ratings (T_a = 25 °C)

Parameter	Symbol	Value	Unit
Peak Repetitive Off-State Voltage [4] (T_J = -40 °C to 110 °C, Sine Wave, 50 to 60 Hz, Gate Open) MCR100-4U MCR100-6U MCR100-8U	V_{DRM}, V_{RRM}	 200 400 600	V
On-State RMS Current (T_C = 80 °C) 180° Conduction Angles	$I_{T(RMS)}$	0.8	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T_J = 25 °C)	I_{TSM}	10	A
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	0.415	A^2s
Forward Peak Gate Power (Pulse Width ≤ 1 µs)	P_{GM}	0.1	W
Forward Average Gate Power (t = 8.3 ms)	$P_{G(AV)}$	0.1	W
Peak Gate Current – Forward (Pulse Width ≤ 1 µs)	I_{GM}	1	A
Peak Gate Voltage – Reverse (Pulse Width ≤ 1 µs)	V_{GRM}	5	V
Operating Junction Temperature Range	T_J	- 40 to + 110	°C
Storage Temperature Range	T_S	- 40 to + 150	°C

Characteristics at T_a = 25 °C

Parameter		Symbol	Max.	Unit
Peak Forward or Reverse Blocking Current [2] at V_D = Rated V_{DRM} and V_{RRM}, R_{GK} = 1 KΩ		I_{DRM}, I_{RRM}	10	µA
Peak Forward On-State Voltage [1] at I_{TM} = 1 A Peak		V_{TM}	1.7	V
Gate Trigger Current [3] at V_{AK} = 7 V, R_L = 100 Ω		I_{GT}	200	µA
Holding Current [2] at V_{AK} = 7 V, Initiating Current = 20 mA	T_C = 25 °C T_C = - 40 °C	I_H	5 10	mA
Latch Current at V_{AK} = 7 V, Ig = 200 µA	T_C = 25 °C T_C = - 40 °C	I_L	10 15	mA
Gate Trigger Voltage [3] at V_{AK} = 7 V, R_L = 100 Ω	T_C = 25 °C T_C = - 40 °C	V_{GT}	0.8 1.2	V

[1] Indicates pulse test width ≤ 1 ms, duty cycle ≤ 1%
[2] R_{GK} = 1 KΩ included in measurement
[3] Does not include R_{GK} in measurement
[4] V_{DRM} and V_{RRM} for all types can be applied on continuous basis. Ratings apply for zero negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

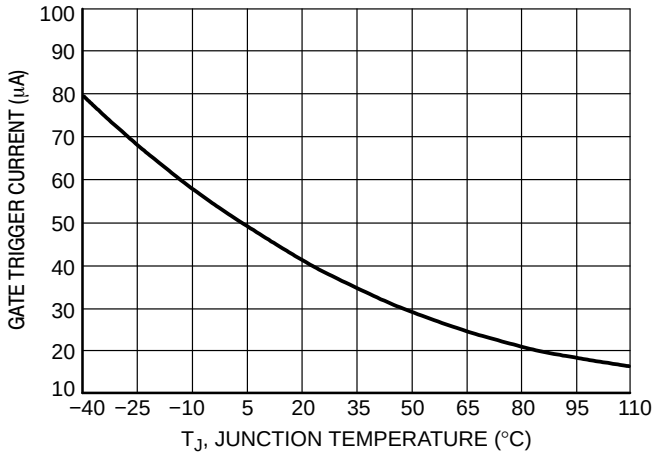


Figure 1. Typical Gate Trigger Current versus Junction Temperature

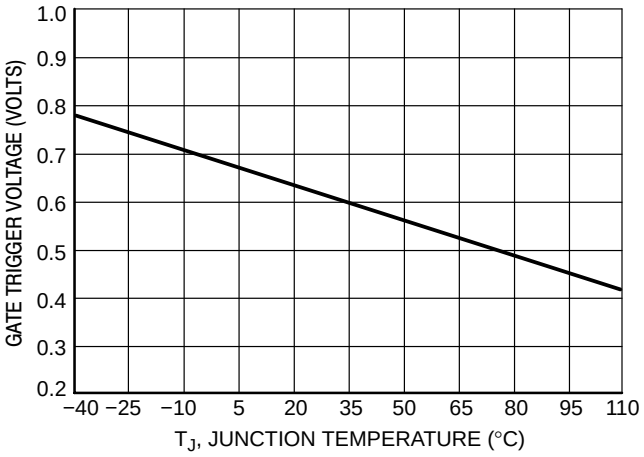


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

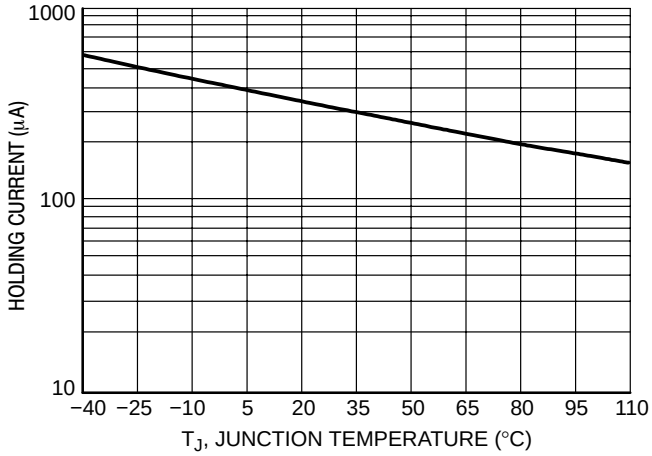


Figure 3. Typical Holding Current versus Junction Temperature

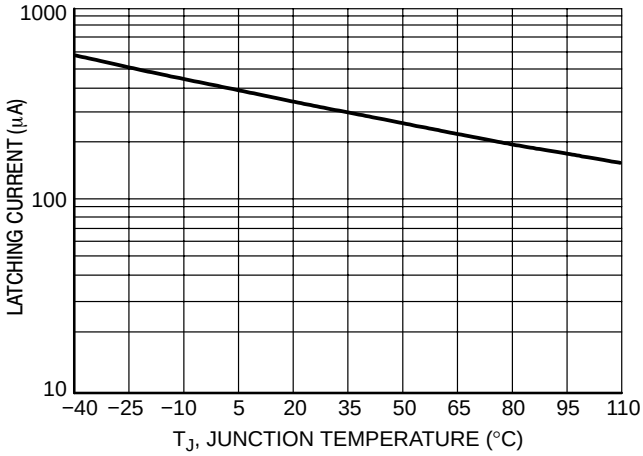


Figure 4. Typical Latching Current versus Junction Temperature

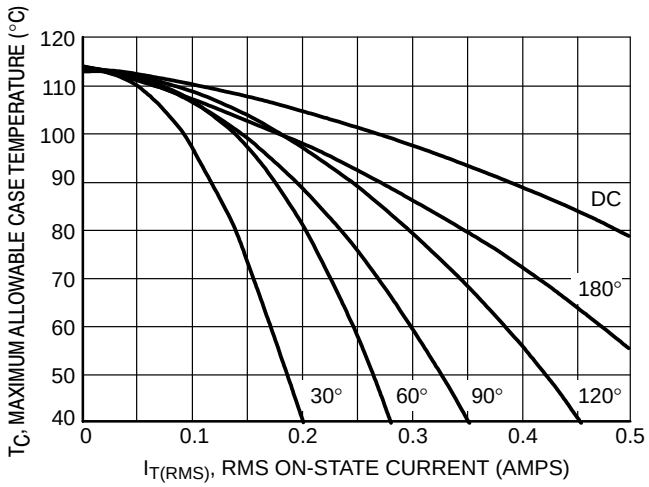


Figure 5. Typical RMS Current Derating

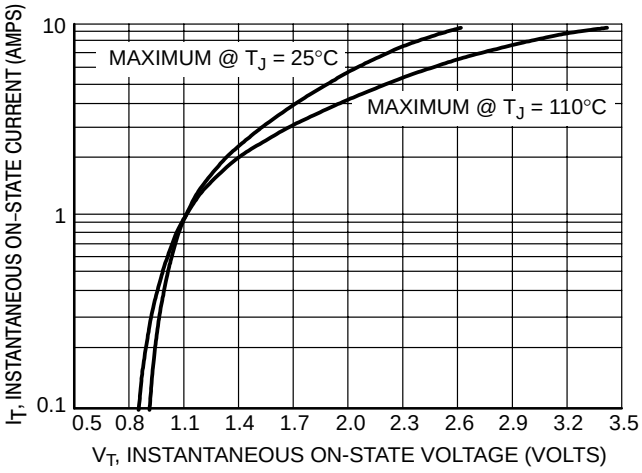
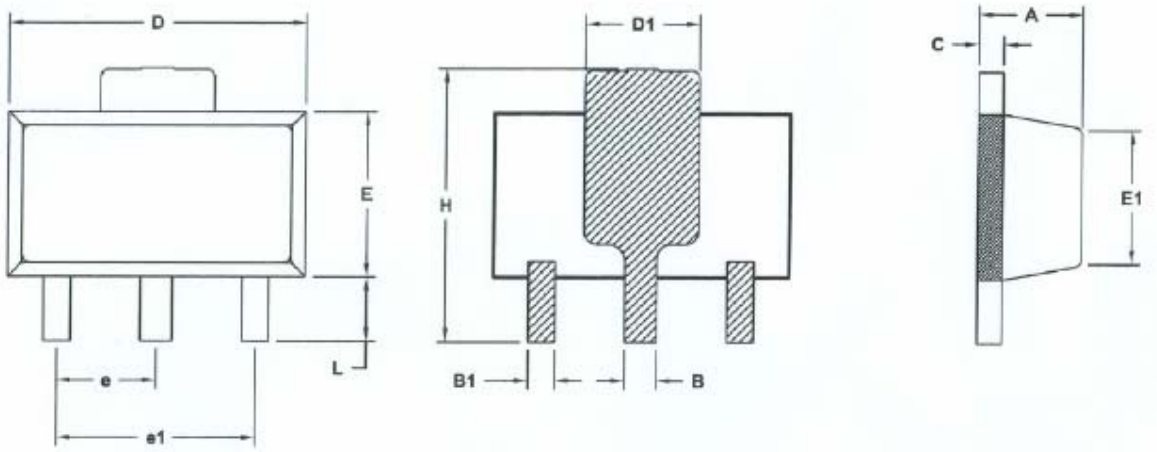


Figure 6. Typical On−State Characteristics

SOT-89 Package Outline Drawing



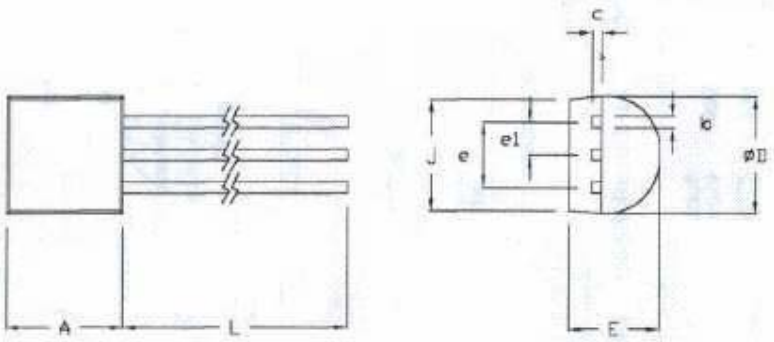
	JEDEC STD POD		CURRENT POD	
	MIN	MAX	MIN	MAX
A	0.055	0.063	0.055	0.063
B	0.017	0.022	0.017	0.022
B1	0.014	0.019	0.014	0.019
C	0.014	0.017	0.014	0.017
D	0.173	0.181	0.173	0.181
D1	0.064	0.072	0.066	0.070
E	0.090	0.102	0.090	0.099
E1	0.084	0.090	0.084	0.086
e	0.059 BSC		0.059	
e1	0.118 BSC		0.118	
H	0.155	0.167	0.155	0.167
L	0.035	0.047	0.035	0.047

NOTE: ALL DIMENSION ARE IN INCHES

NOTE:

1. TOP PACKAGE ANGLE IS 9° +1°/-2° TOLERANCE. BOTTOM PACKAGE ANGLE IS 3° MAX.
2. PACKAGE CORNER RADIUS IS 5 MILS MAX ON ALL CORNERS.
3. SHINNY PACKAGE FINISH ON ALL SIDES EXCEPT TOP SIDE FINISH IS MINIMUM MATTE OF 10-14VDI.

TO-92 Package Outline Drawing



JEDEC

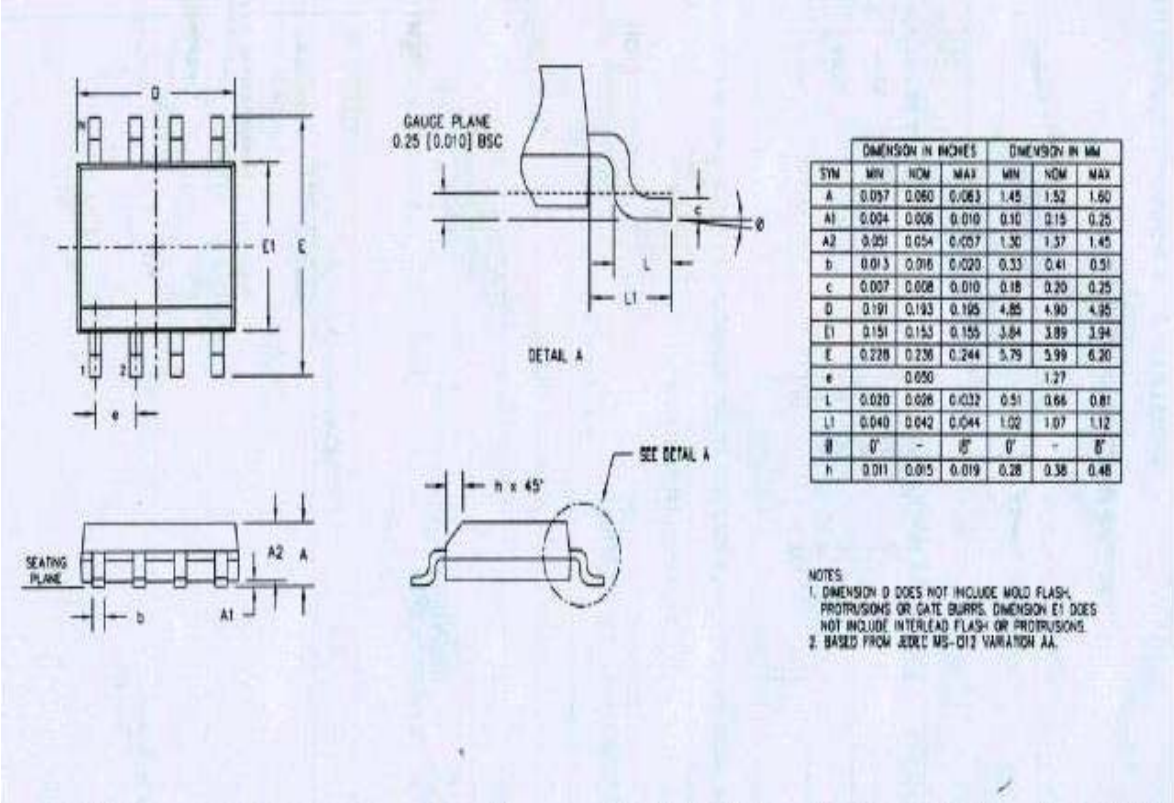
SYMBOL	INCHES	
	MIN	MAX
A	0.170	0.210
b	0.015	0.022
c	0.014	0.020
ØD	0.175	0.205
e	0.095	0.105
e1	0.045	0.055
E	0.125	0.165
J	0.135	-
L	0.500	-

NOTE : BASE FROM THE JEDEC STANDARD TO-226 ISSUE G

CIRTEK

SYMBOL	INCHES		
	MIN	MAX	ACTUAL
A	0.178	0.182	0.180
b	0.015	0.020	0.018
c	0.014	0.016	0.015
ØD	0.178	0.182	0.180
e	0.098	0.102	0.100
e1	0.048	0.052	0.050
E	0.138	0.142	0.140
J	0.168	0.174	0.171
L	0.500	0.570	0.550

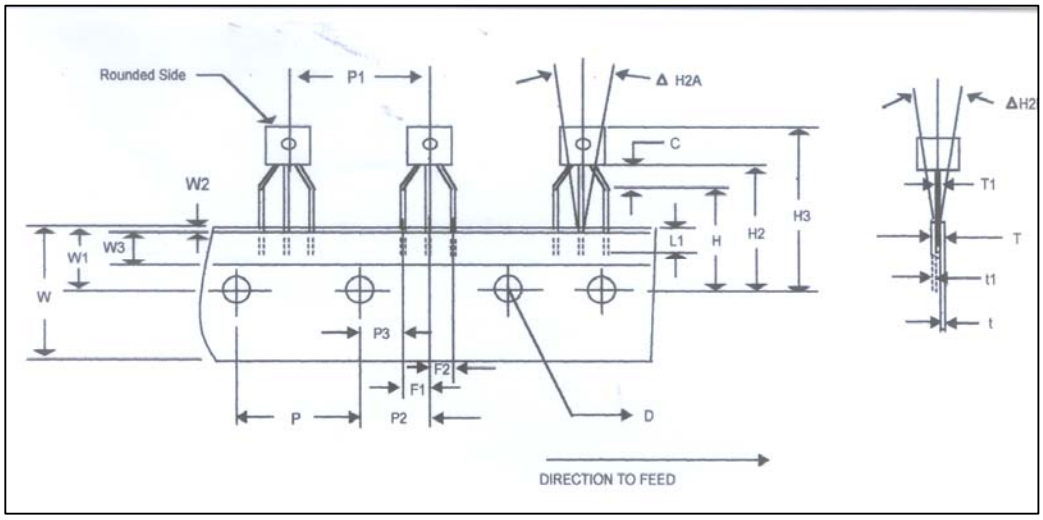
SOIC 8L Package Outline Drawing



	DIMENSION IN INCHES			DIMENSION IN MM		
SYM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.057	0.060	0.063	1.45	1.52	1.60
A1	0.004	0.006	0.010	0.10	0.15	0.25
A2	0.051	0.054	0.057	1.30	1.37	1.45
b	0.013	0.016	0.020	0.33	0.41	0.51
c	0.007	0.008	0.010	0.18	0.20	0.25
D	0.191	0.193	0.195	4.85	4.90	4.95
E1	0.151	0.153	0.155	3.84	3.89	3.94
E	0.228	0.236	0.244	5.79	5.99	6.20
e		0.050			1.27	
L	0.020	0.026	0.032	0.51	0.66	0.81
L1	0.040	0.042	0.044	1.02	1.07	1.12
θ	0°	-	8°	0°	-	8°
h	0.011	0.015	0.019	0.28	0.38	0.48

NOTES:
1. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
2. BASED FROM JEDEC MS-012 VARIATION AA.

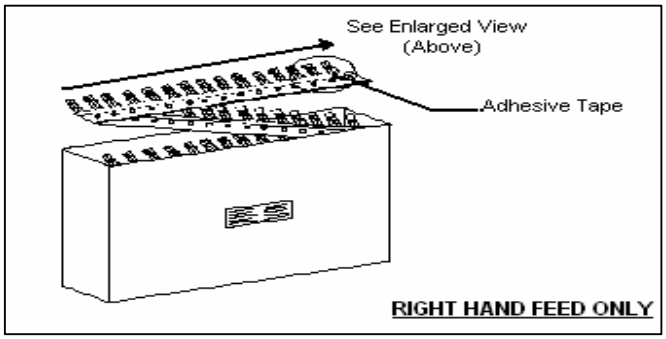
TO-92 Taping Specifications



SYMBOL	DESCRIPTION	NOMINAL VALUE		TOLERANCES MIN		MAX	
		mm	inch	mm	inch	mm	inch
C	Bottom of Component to seating Plane	2.50	0.098	1.5	0.059	4.00	0.157
D	Feed Hole Diameter	4.0	0.157	3.8	0.150	4.2	0.165
F1/F2	Lead Pitch (Left/ Right)	2.54	0.100	2.4	0.094	2.8	0.110
H	Height of Seating Plane	16	0.630	15.5	0.610	16.5	0.650
H2A	Deflection (Left or Right)	0.50	0.020	0	0	0.50	0.020
H2B	Deflection (Front or Rear)	1.0	0.039	0	0	1.0	0.039
H2	Feed Hole to Bottom of Component	18.75	0.738	18.00	0.709	19.5	0.768
H3	Feed Hole Center to Overall Transistor Height	23.32	0.918	22.52	0.887	24.12	0.949
L	Defective Unit Clipped Dimension	-	-	-	-	11	0.433
L1	Leadwire Enclosure	2.50	0.098	2.50	0.098	-	-
P	Feed Hole Pitch	12.7	0.500	12.40	0.488	13.0	0.512
P1	Center Lead to Center Lead	12.7	0.500	12.2	0.500	13.2	0.520
P2	Center of Feed Hole to Center Lead	6.35	0.250	6.0	0.234	6.75	0.266
P3 (P2-F1)	First Lead Spacing Dimension	3.75	0.148	3.6	0.142	3.95	0.156
T(t+t1+T1)	Overall Taped Package Thickness	-	-	-	-	1.55	0.061
W1	Edge to Sprocket Hole Center	9.0	0.354	8.50	0.335	9.50	0.374
W2	Adhesive Tape Position	0.3	0.010	0	0	0.50	0.020

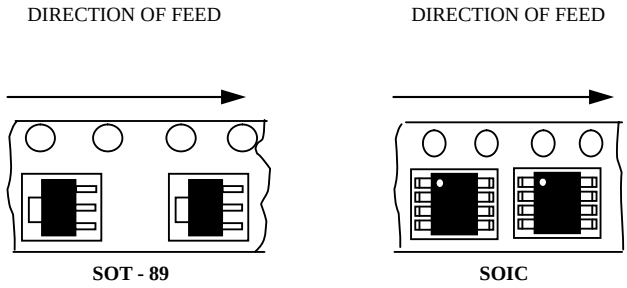
Note:T1 refer to T0-92 POD letter b
W refer tocarrier tape specs section 7.2.3.4.3
W3 refer to adhesive tape specs section 7.2.4.4
t refer to carrier tape specs section 7.2.4.3

- **Standard Taping Style (Ammo Pack)**

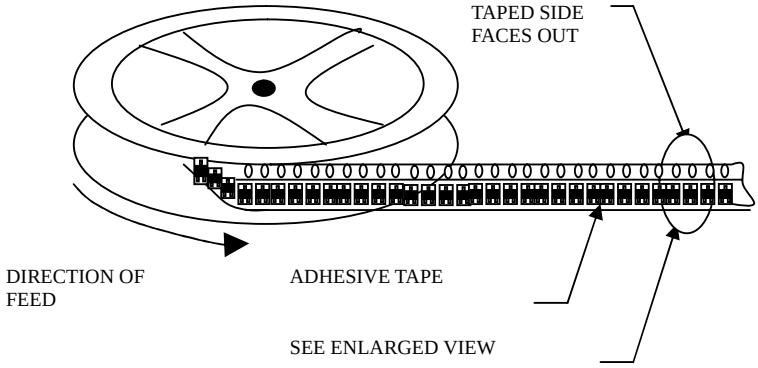


Surface Mountable Tape and Reel Specifications

- **PART ORIENTATION**



- **REEL ORIENTATION**



- **TAPE and REEL GUIDELINES**

Package Type	Std. Qty per Reel	Embossed Carrier Tape	Cover Tape	Heat/Temp Setting	Sealing Pressure	Taping Speed	Tape Leader/Trailer	Take-up Reel Size	Peel Strength
8L NB SOIC	2500	AC90.0P2	ABX0133 (13mm)	146 +/-3 ºC	15 to 35 psi	2-4 mm/sec	18” to 22”	13”Ø	20 to 70 gram force
8L NB SOIC	2500	S08.CP	-						
8L NB SOIC	2500	S08NP2 CL3 22B3 L90 W12	9.2MM						
8L NB SOIC	2500	-							
SOT-89	2500	-	ABX0133 (13.3mm)						
		SOT89 C.P	-						

Note: **Embossed Carrier Tape and Cover Tape is depending on SLI supplier.**