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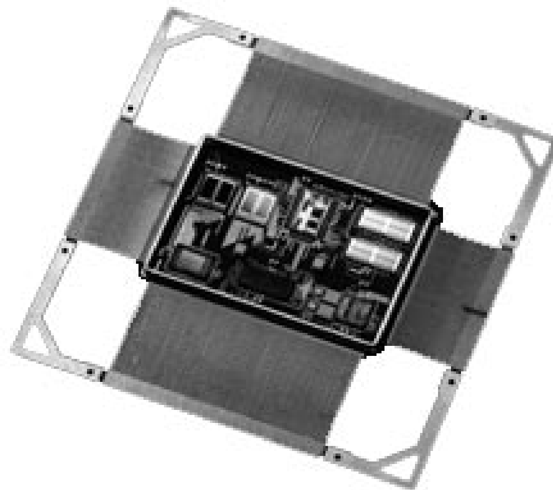
The Future in Microelectronics
CIRCUIT TECHNOLOGY

APPLICATION NOTE #100

A Proposal for the Design and Manufacture of a High Speed CPU Multichip Module for GHz Signal Processing



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1.0 Technical Description

Aeroflex is proposing a thin film MCM, type “D” configuration for High Speed CPU Multichip Module for GHz Signal Processing. The following is a description of a module with similar technologies to those that will be used to meet the 1GHz data processing speed. Also presented is the rationale for the use of the materials and processes indicated.

1.1 HASP Module

As an example of a comparative MCM, the HASP module was chosen. The HASP (Hybrid Associative String Processor) module as illustrated in Figure 1, was designed and manufactured by our MCM design specialist, John Reche. Mr. Reche is a consulant associated with Aeroflex in the design and development of advanced MCM packaging technologies.

The HASP module contains 16 microprocessor die that operate in a parallel processor mode to achieve 700 million operations per second. This module is designed to operate a 60 mHz clock speed. It contains the following additional devices: 16 each of a 20R4 PAL, 2 each of a 22VlO PAL, and 12 each of a 74FC type transceiver in addition to decoupling capacitors. The technology used is silicon die on a silicon substrate, with thin film copper conductors in a polymer insulating medium. The power dissipation is approximately 20 watts in a 2.5” by 2.5” package. When sixteen of these modules are combined together they can perform 12.6 giga-operations (32 bit additions) at a clock frequency of 60 MHz.

The proposed High Speed CPU module will use the same technologies (as described below) except for the substrate material, which will be changed from silicon to aluminum nitride. The aluminum nitride has twice the thermal conductivity of silicon.

1.2 Basic MCM Material Technologies

The CPU MCM will use a combination of advanced substrate and dielectric materials to meet the requirements of circuit density, clock speed, power dissipation and low cost. The basic module will consist of an aluminum nitride substrate supporting an ultrafine line MCM-D circuit. A multilayer conductor pattern of copper, interconnects the semiconductor devices via controlled impedance transmission lines. This technology is known as high density multilayer interconnect (HDMI). This process has successfully been used to construct up to a six metallization layer MCM substrate structure. The proposed multichip module will be fabricated on the aluminum nitride substrate by a deposition process with a polymer, bisbenzocyclobutene (BCB) for dielectric layers and the copper for die interconnections. BCB is the polymer of choice because of its low dielectric constant (2.70) and low water absorption. A ceramic cover will be bonded over the completed circuit for mechanical protection. Leads will be available on up to four sides for surface mounting.

1.2.1 Aluminum Nitride Substrate

Aluminum nitride (AlN) is used as the substrate and bottom of the package because it is a highly efficient thermal conductor with a thermal conductivity of 170 W/mK, slightly less than that of

HASP MCM DEMONSTRATOR

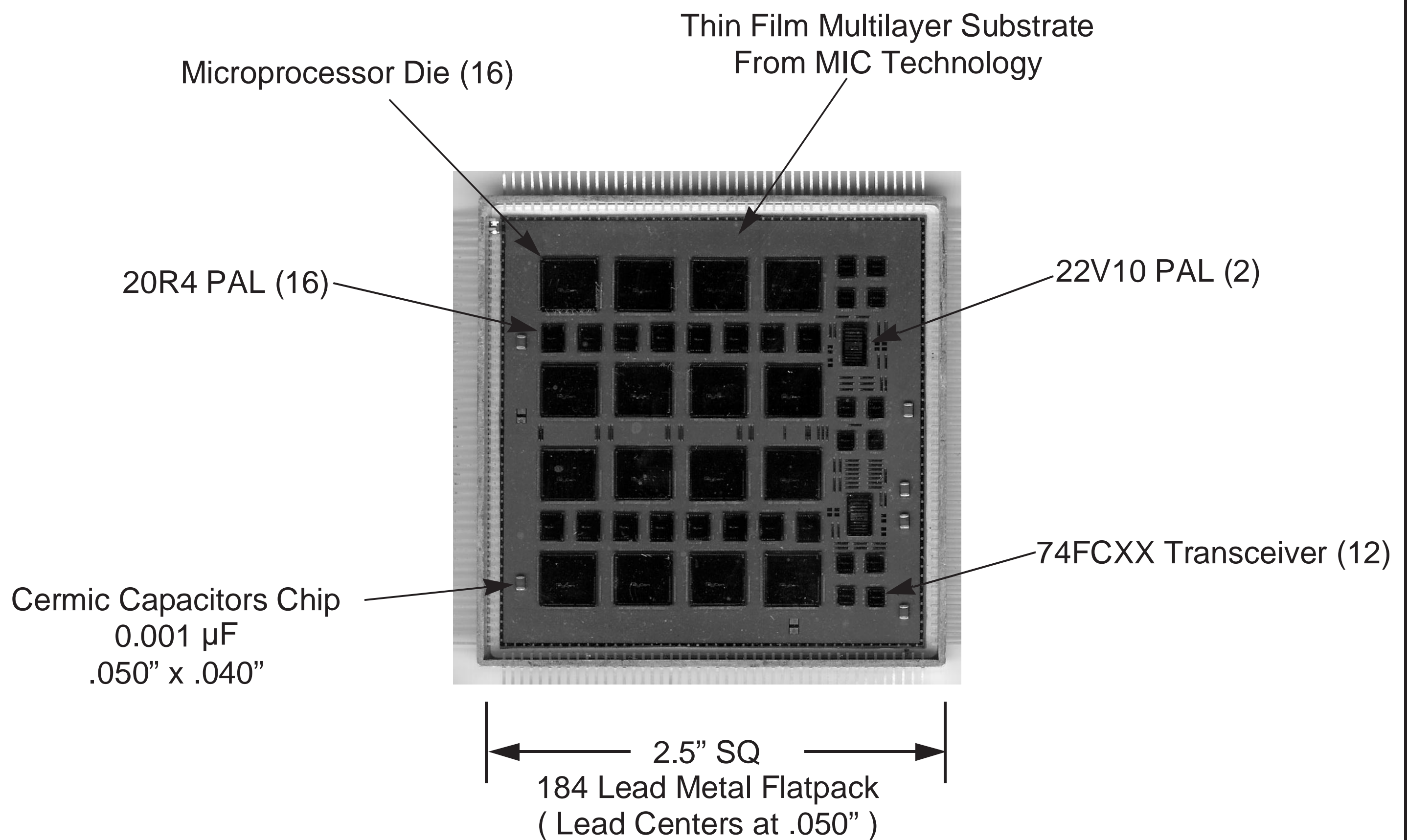


Figure 1

beryllium oxide. By attaching the die directly to the aluminum nitride substrate, heat transfer is optimized (see page 6, MCM Thermal Analysis).

Aluminum nitride has several other advantages, they are:

- The coefficient of thermal expansion of the AlN substrate is very close to that of the silicon die, thus preventing die bond failures that could occur under thermal cycling conditions.
- The dielectric constant and electrical resistance are similar to aluminum oxide.
- The material has a higher bending strength which makes for a stronger package.
- The basic blank substrate material is available from several sources at reasonable prices.

1.2.2 Copper conductor patterns

The advantages of using copper over other conductor materials such as aluminum or tungsten are well known. The use of copper reduces resistive losses, improves rise time and reduces pulse delay. Typical line widths range from 2.5 microns to 25 microns for very dense packing of components.

1.2.3 Bisbenzocyclobutene (BCB) Insulator layers

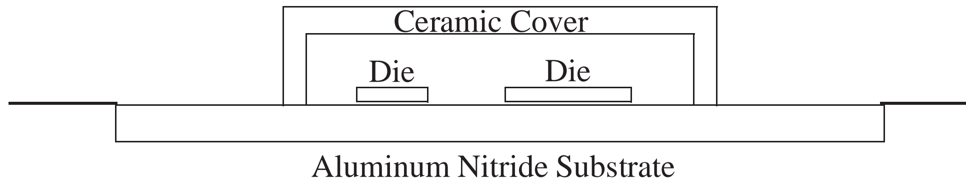
From transmission line theory, the propagation delays in a transmission line structure are inversely proportional to the square root of the dielectric constant. Therefore it is advantageous to use lower dielectric constant materials to build MCMs that must operate at very high frequencies. The use of a bisbenzocyclobutene polymeric insulator material with a relatively low dielectric constant of 2.7, is a major factor in the design of the CPU MCM. The BCB material will support clock frequencies well above 1000mHz. This is a substantial improvement over dielectrics normally used in multichip modules such as, alumina or polyimide, whose dielectric constants range from a high of 11 to a low of 3.4. The BCB material also has the advantage of low water absorption which reduces high frequency losses, improves efficiency and reduces heating effects. The use of BCB permits practical line widths and conductor spacing that can be used to attain characteristic impedance values in the range of 50 Ohms to 75 Ohms which matches standard semiconductor requirements.

1.3 Die interconnections

For reasons of cost and delivery, the initial units will be designed with gold or aluminum wire bonding. This technology is usable up to 1 GHz clock frequencies and permits quick assembly of preproduction units with little extra tooling charges. Eventually, when production quantities are generated, a conversion to tape automated bonding (TAB) will be employed to reduce costs and speed deliveries. The TAB permits improved die testing and is very conducive to automatic assembly. TAB will also improve the frequency response of the MCM by reducing lead bond inductance.

1.3.1 Package Sealing

As illustrated in the following package cross section, the basic package consists of the substrate covered with a ceramic cover to prevent damage to the die and provide a seal against dust and humidity. The leads are placed at the AlN substrate edge, where they can be shaped for surface mount or plug in applications.



1.4 Thermal Design

1.4.1 Thermal Management

The thermal management of the MCM is facilitated in two ways - first, by partially eliminating power consumption in the circuit, and second, by allowing the use of substrates and packages which dissipate the heat better. The lower capacitance of the Aeroflex design translates in a proportional reduction of power dissipation. The power dissipated in the interconnections between the die is:

$$\mathrm{POWER} = \left(\frac{1}{2}\right) \times f \cdot (CV^2)$$

where *f i*s the clock frequency, *C* is the line capacitance, and *V* is the logic voltage swing. A substantial portion of total circuit power dissipation in typical circuits is used to charge and discharge the line capacitance due to inter-chip voltage swings. In modern MCMs, it is reasonable to expect a reduction in line capacitance by at least an order of magnitude over printed circuit boards in a typical digital circuit.

As a consequence of reduced line capacitance, it is possible to reduce the power dissipation of ASIC logic line drivers. It is estimated that an average of 50% of the power dissipated in a chip is dissipated on the periphery by the line drivers. Line drivers are normally designed to handle long traces on PC boards. Many circuits developed for MCM technology can have reduced power dissipation at the line driver level because they can use ASICs which can be tailored to the purpose.

In addition,the substrate material can be optimized to dissipate larger amounts of power per unit area and closely match the coefficient of expansion of large size semiconductor dies. The increased packaging density of MCMs requires better heat conduction capability than the older hybrid technology required. Alumina ceramic is no longer suitable because its coefficient of expansion is too high (which would stress large dies attached to it) and its thermal conduction is poor. Aluminum nitride will be used because it has excellent electrical insulating properties, good heat conduction and a matching thermal coefficient of expansion.

1.4.2 MCM Thermal resistance

The figure on the next page presents the thermal resistance calculations of the internal semiconductor die to the outside of the module. A calculation was made to determine the thermal resistance from the semiconductor junction to the case, or Ø J-C. This calculation assumes no heat spreading, which is a conservative assumption that will result in a higher than actual thermal resistance. A smaller surface area die will have a higher thermal resistance, all other factors being equal.

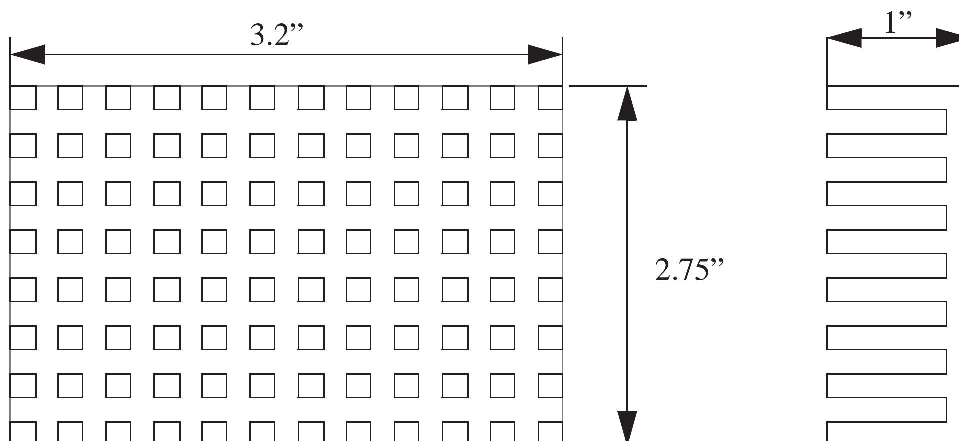
The calculation involves three layers of material, the silicon die, the die adhesive, and the aluminum nitride case substrate. The die bonding method and adhesive used does not cause voids under the die, so the effects of voids will be neglected. The calculated thermal resistance for the 0.431 inch square die is 0.178 C°/W, and the 0.300 inch square die is 0.368 C°/W. This calculation is based on a uniform heat source (the same heat flux density) applied across the semiconductor die. This calculation will accurately determine the thermal resistance if all the die have about the same power dissipation per unit of surface area, since there will be no thermal effects from one die on any another. If however, any die has a higher power dissipation per unit area, this higher dissipating die will represent the worst case temperature condition, and thus limit the maximum junction temperature rise for a given maximum case temperature. This simplified analysis will also apply in this situation, since the hotter die will create a heat spreading effect, which results in a lower thermal resistance. While it is true that this hotter die will tend to increase the thermal resistance of nearby lower power density devices, in reality the hotter die will be the worst case.

In modern multichip modules which use microprocessors, large ASICs and memory devices, die dimensions are typically ten to twenty times the substrate thickness. Under these conditions,because of the large surface area to thickness ratio, most of the heat flows downward to the heat sink and heat spreading is kept to a minimum.

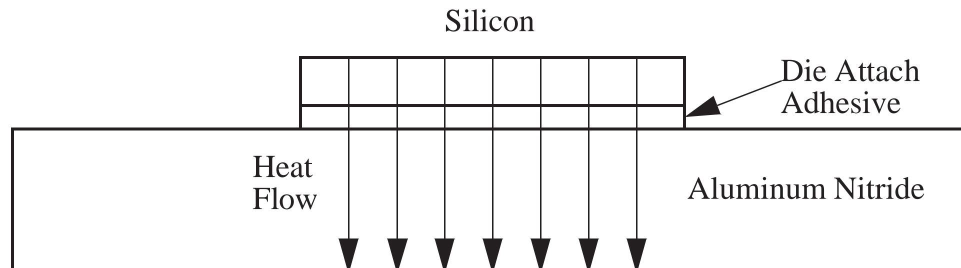
When the MCM is designed, a more through finite element thermal analysis will be performed on the actual configuration to confirm these approximations.

1.4.3 Heat Sink Thermal Resistance

The following heat sink, cooled by forced air as shown in the chart on page 7, will maintain the MCM die junction temperatures below 85°C with the die power dissipations as indicated.



Multichip Module Die Thermal Analysis



Thermal Resistance calculation

Thermal resistance in C°/W= Thickness/(Thermal conductivity)(Area)

Note: All dimensions in Inches

1. Silicon die, 0.020 inches thick x 0.431 inches square

   Øs = 0.20/(2.13)(0.431)(0.431)

   Øs = 0.051 C°/W

2. Die Adhesive, 0.002 inches thick

   Øa = 0.002/(0.14)(0.431)(0.431)

   Øa = 0.076 C°/W

3. Aluminum Nitride Substrate, 0.40 inches thick

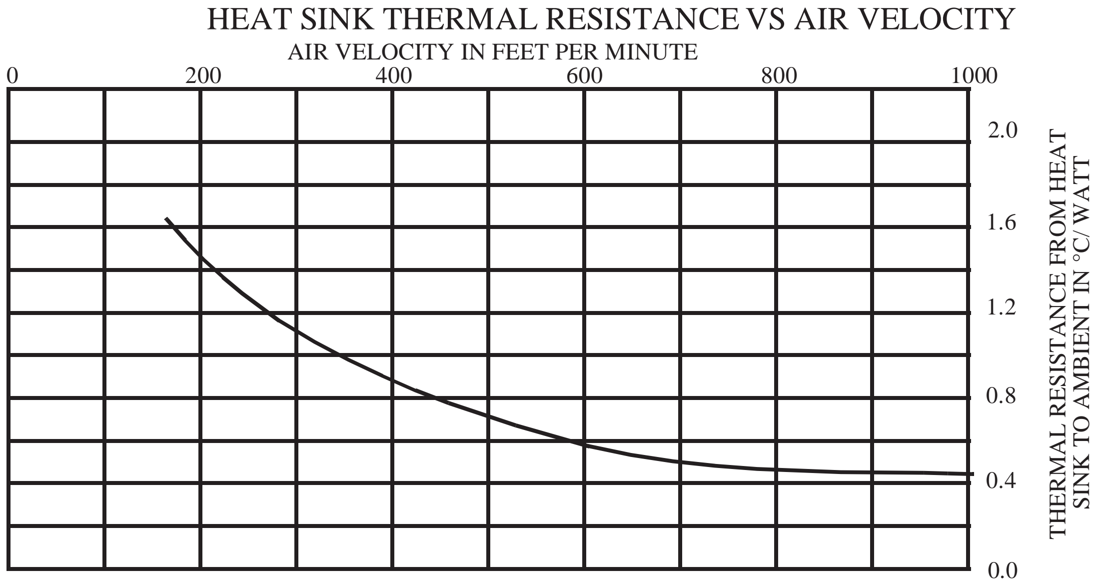
   Øal = 0.040/(4.25)(0.431)(0.431)

   Øal = 0.051 C°/W

Total Thermal resistance = 0.178 C•/W;

For the *smaller die*, 300 mils in size, all thicknesses remain the same, the thermal resistance is calculated to be ***0.368 C•/W***

Characteristics of the heat sink in terms of thermal resistance vs. air velocity are shown below:



This heat sink is to be mechanically attached to the MCM case. Sufficient pressure (at least 10 pounds/ sq inch) and conductive joint compound is used to make intimate thermal contact to the case. The estimated temperature rise can be determined by the thermal resistance and as follows:

Temperature Rise	Module Die	
Sizes	0.431"X 0.431"	0.300" x 0.300"
Junction of die to case	0.178 °C/W x 15W = 2.67 °C	0.368 °C/W x 15W= 5.52 °C
Case to heat sink	0.200 °C/W x 25W = 5.00 °C	0.200 °C/W x 25W= 5.00 °C
Heat sink to ambient, (air velocity 300ft/min)	1.100 °C/W x 25W =27.50 °C	1.100 °C/W x 25W=27.50 °C
Total, junction to ambient	35.17°C	37.02°C

The temperature rise of 37°C is within the required 85 °C maximum junction temperature, if a maximum ambient temperature of 45°C is assumed.

Please note that these values of temperature rise are conservative since they do not assume any other mode of heat transfer. In reality, the die are cooled by the following additional means:

- Conduction through the die bond wires or tab connections.
- Internal module air convection from the die to the case and air convection around the case.
- Heat spreading conduction from the edge of the die to the substrate.
- Radiation from the die to the case, and from the case to the heat sink and air.
- Heat capacity storage effects of the substrate and heat sink, if the duty cycle is less than 100%.

2.0 Conclusion

Aeroflex has proposed a thin film MCM, type "D" configuration for High Speed CPU Multichip Module for GHz Signal Processing in this application note. The technology to develop MCMs that can be used to meet GHz data processing speed is now available for commercial and military products. For your specific needs please contact our MCM application representative.