MC34063C
DC to DC Converter Control Circuits

DESCRIPTION

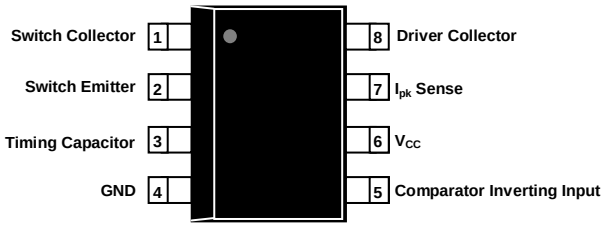
The MC34063C is a monolithic control circuit containing the primary functions required for DC-to-DC converter. This device consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. The MC34063C was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

FEATURES

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

PIN CONFIGURATION – Top View

8L SOIC



PACKAGE TOP MARKING:
(For 8L SOIC)

MC34063 FYMXXXS GYYWW

Line 1: Device
Line 2: Lot No. Code
F – Foundry Code (C)
YMXXX – 5 Character Lot No.
S – Split Code
Line 3: Date Code
G – Assembly Vendor Code
YY – Year
WW – Workweek

ORDERING INFORMATION

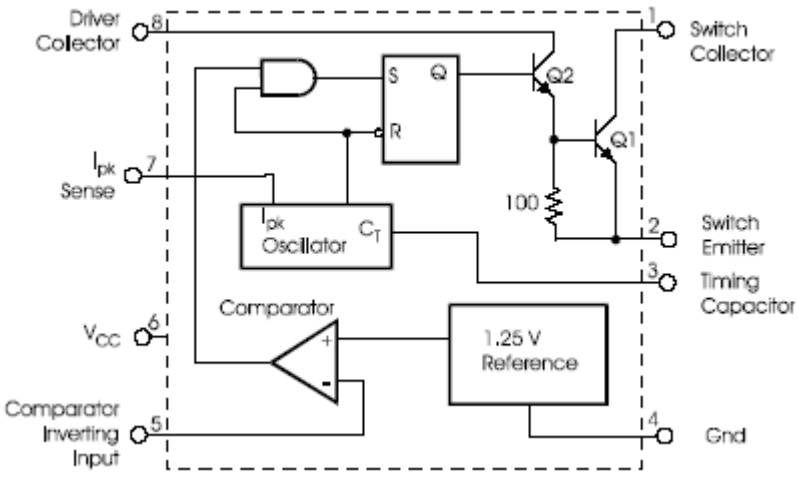
MC34063C D8 13

Circuit Type:
DC to DC Converter
Control Circuits

Package Style:
D8 = SOIC/8L

Packaging Option:
T = Tube
13 = Tape and Reel (13" Reel Dia)

SCHEMATIC DIAGRAM – Bottom View



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	-0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage (V_{PIN1} = 40 V)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	A
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	0 to +125	°C
Storage Temperature Range	Tstg	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V, Ta = T_{low} to T_{high}, unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (V_{pin5} = 0V, C_T = 1.0 nF, T_A = 25°C)	f_{osc}	24	33	42	kHZ
Charge Current (V_{CC} = 5.0V to 40V, T_A = 25°C)	I_{chg}	24	35	42	µA
Discharge Current (V_{CC} = 5.0V to 40V, T_A = 25°C)	I_{dischg}	140	220	260	µA
Discharge to Charge Current Ratio (Pin 7 to V_{CC}, T_A = 25°C)	I_{dischg}/ I_{chg}	5.2	6.5	7.5	-
Current Limit Sense Voltage (I_{chg} = I_{dischg}, T_A = 25°C)	$V_{Ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (NOTE 2)					
Saturation Voltage, Darlington Connection (I_{SW} = 1.0 A, Pins 1, 8 connected)	$V_{CE(sat)}$	-	1.0	1.3	V
Saturation Voltage, Darlington Connection (I_{SW} = 1.0 A, $R_{pin\ 8}$ = 82Ω to V_{CC}, Forced β ≡ 20)	$V_{CE(sat)}$	-	0.45	0.7	V
DC Current Gain (I_{SW} = 1.0 A, V_{CE} = 5.0 V, TA = 25 °C)	h_{FE}	50	75	-	-
Collector Off-State Current (V_{CE} = 40 V)	$I_{C(off)}$	-	40	100	µA
COMPARATOR					
Threshold Voltage (T_A=25°C) (T_A=T_{low} to T_{high})	Vth	1.225 1.21	1.25 -	1.275 1.29	V
Threshold Voltage Line Regulation (V_{CC}=3.0 V to 40 V)	Reg_{line}	-	1.4	5.0	mV
Input Bias Current (V_{in}=0 V)	I_{IB}	-	-20	-400	nA
TOTAL DEVICE					
Supply Current (V_{CC} = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, Vpin 5 > Vth, Pin 2 = Gnd, remaining pins open)	I_{CC}	-	-	4.0	mA

Notes:

1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 1. Output Switch On-Off Time versus Oscillator Timing Capacitor

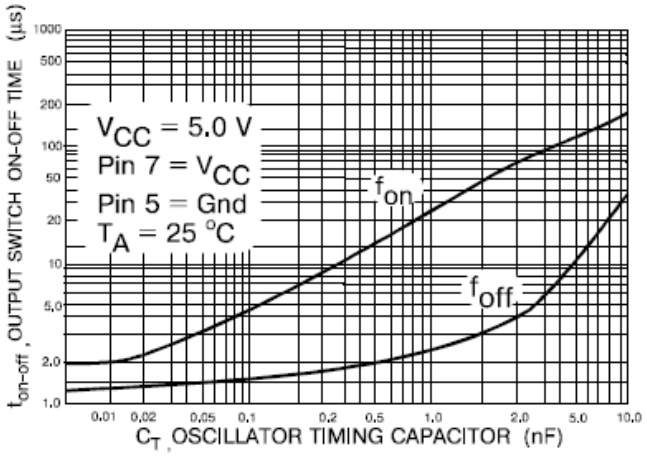


Figure 2. Timing Capacitor Waveform

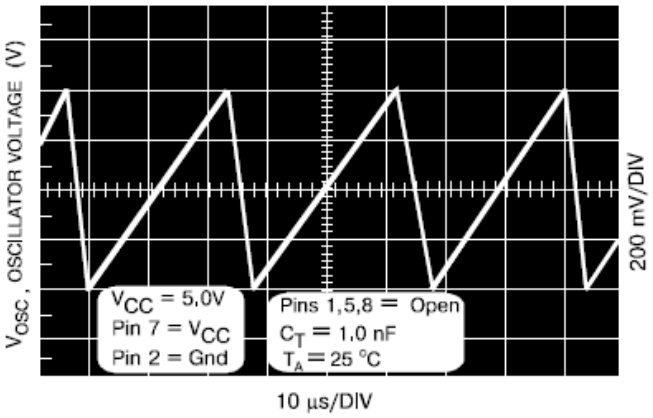


Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

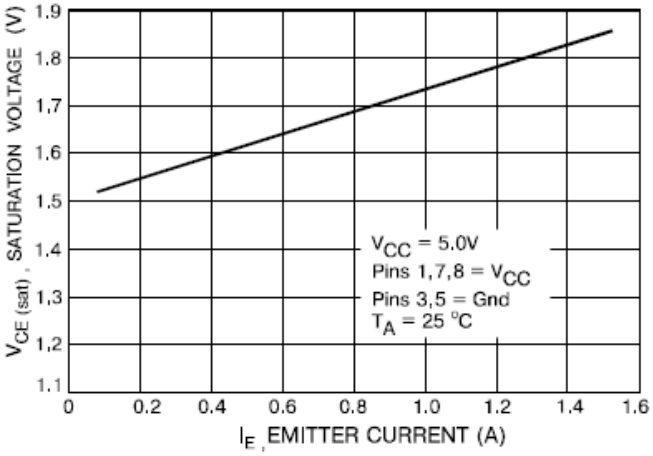


Figure 4. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

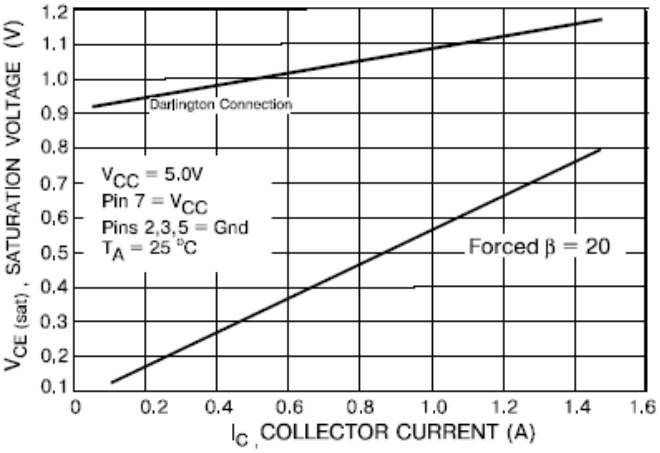


Figure 5. Current Limit Sense Voltage versus Temperature

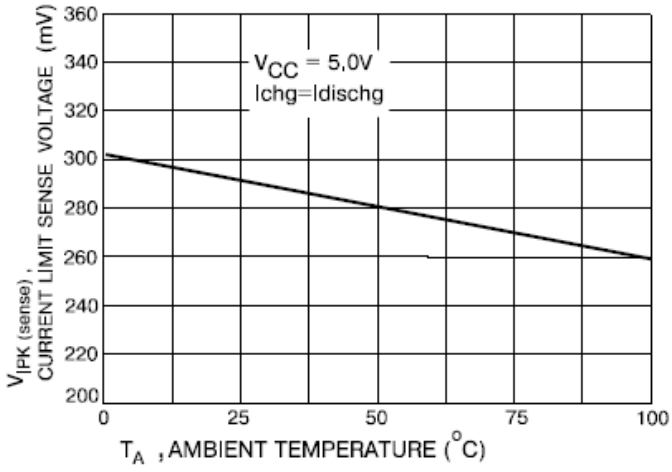
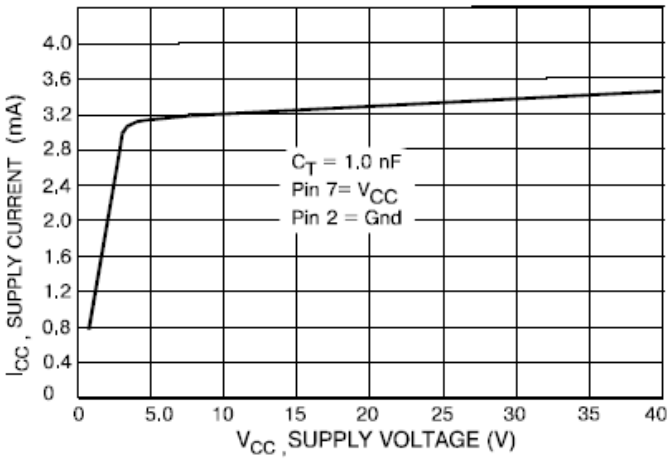


Figure 6. Standby Supply Current versus Supply Voltage



APPLICATION INFORMATION

Figure 1. Step-up Converter

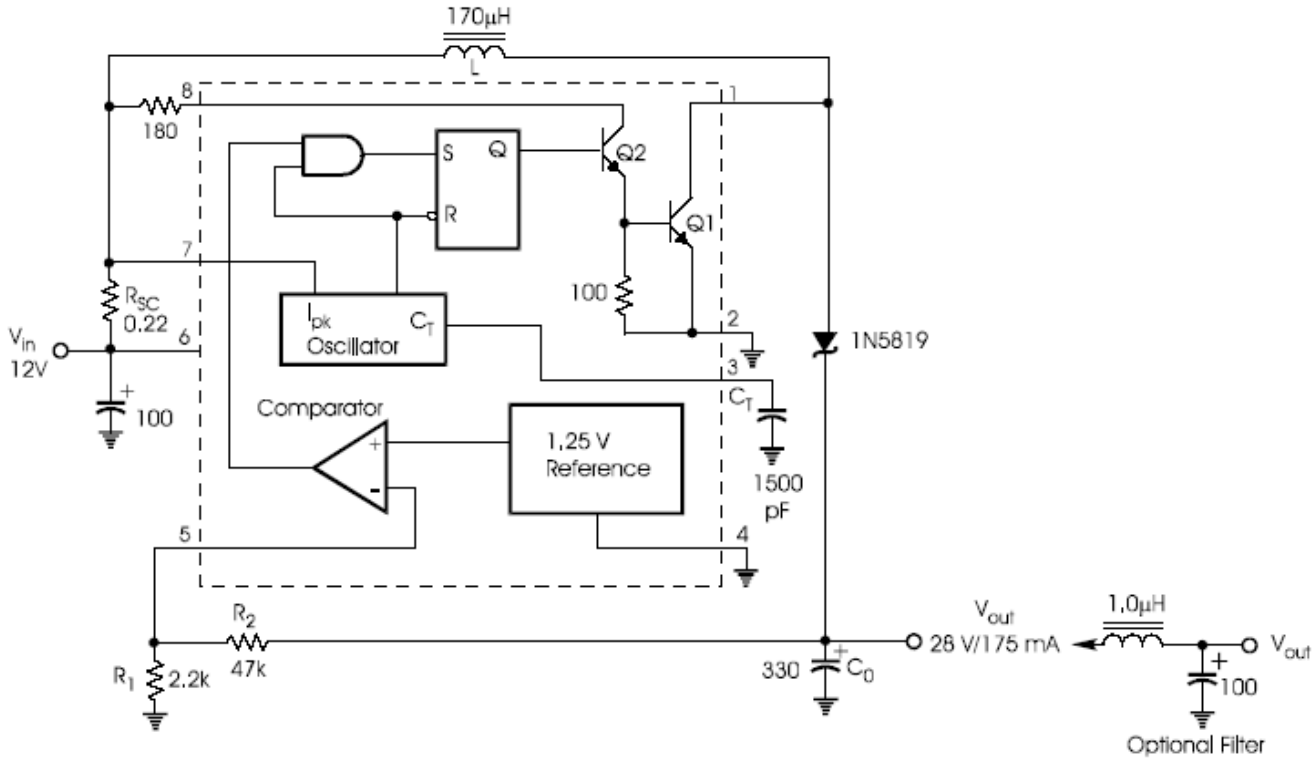


Figure 2. External Current Boost Connections for I_C Peak Greater than 1.5 A
2a. External NPN Switch **2b. External NPN Saturated Switch**

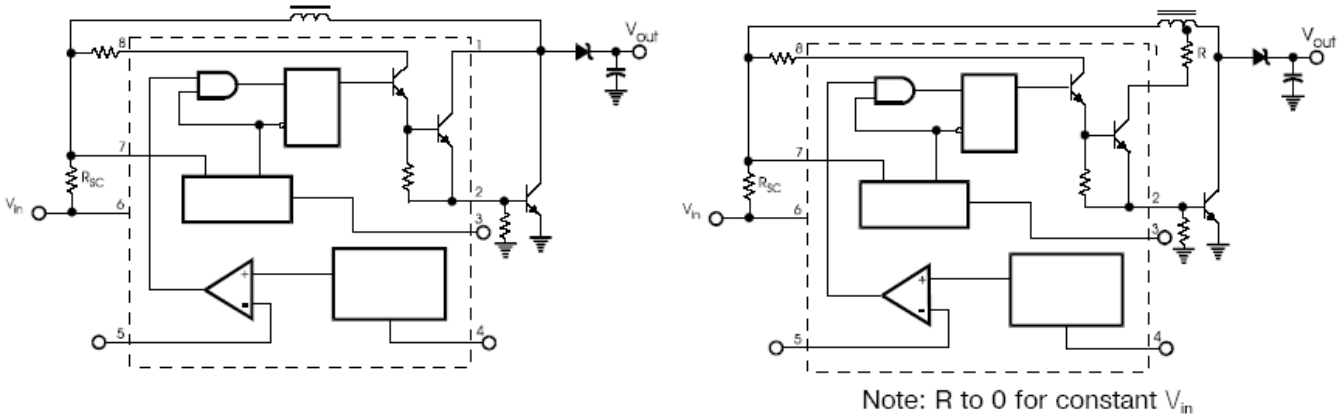


Figure 3. Step-Down Converter

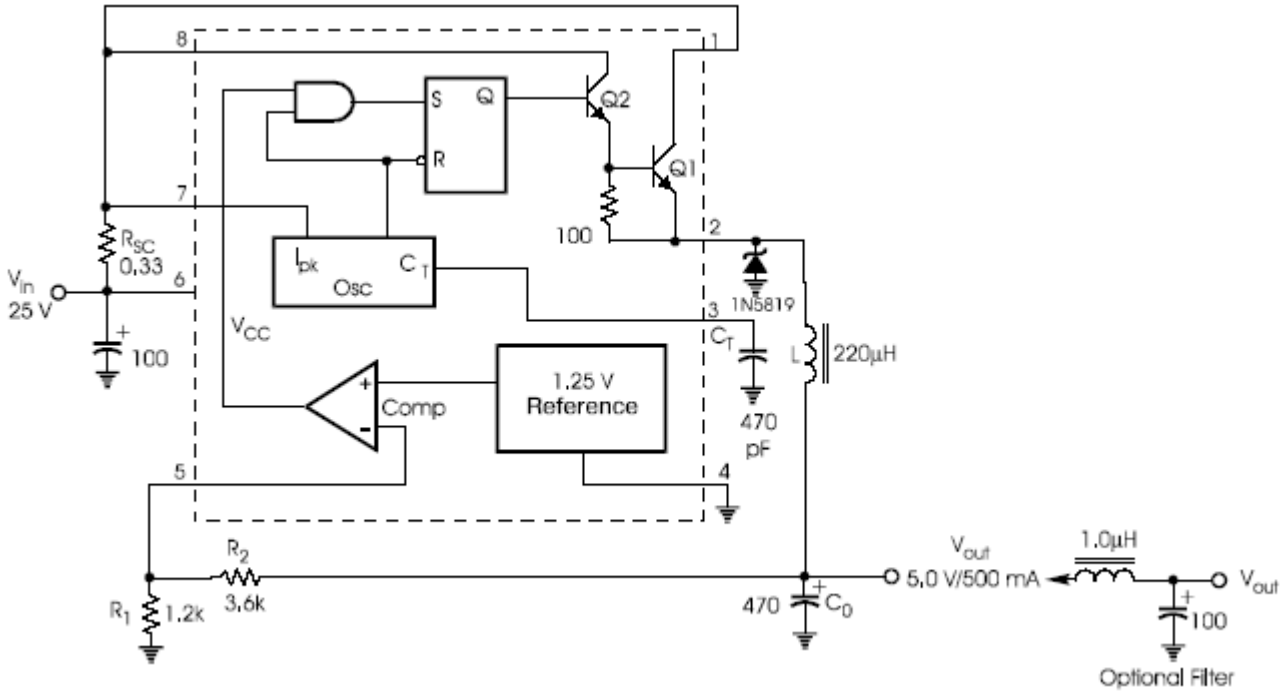


Figure 4. External Current Boost Connections for I_C Peak Greater than 1.5 A
4a. External NPN Switch **4b. External PNP Saturated Switch**

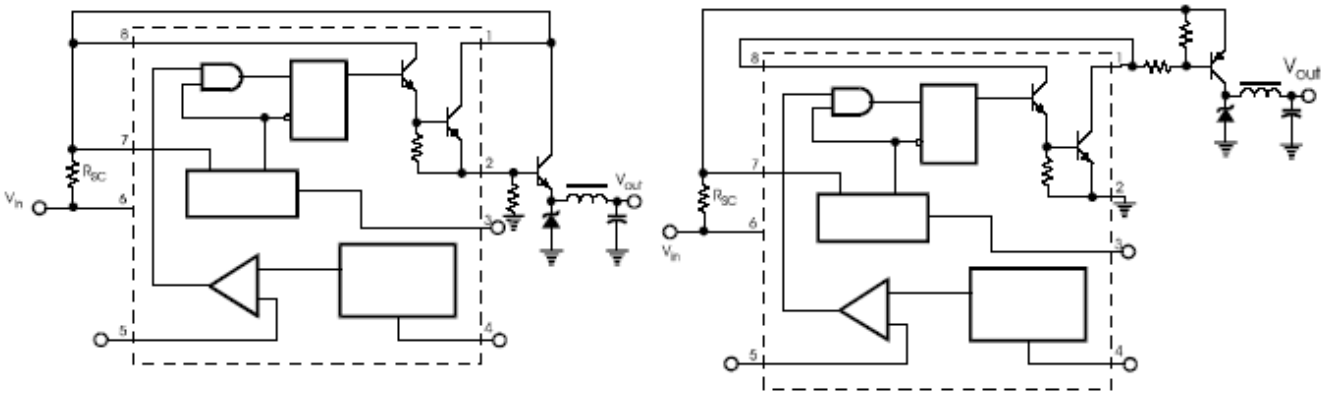


Figure 5. Voltage Inverting Converter

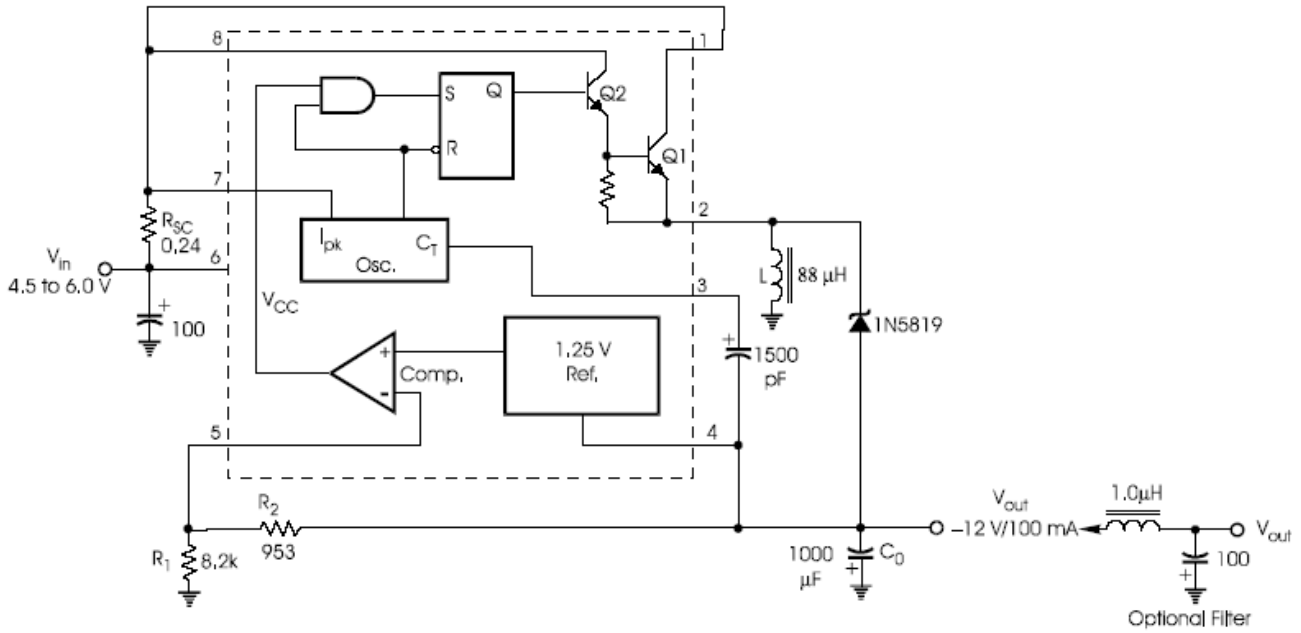


Figure 6. External Current Boost Connections for I_C Peak Greater than 1.5 A
6a. External NPN Switch **6b. External PNP Saturated Switch**

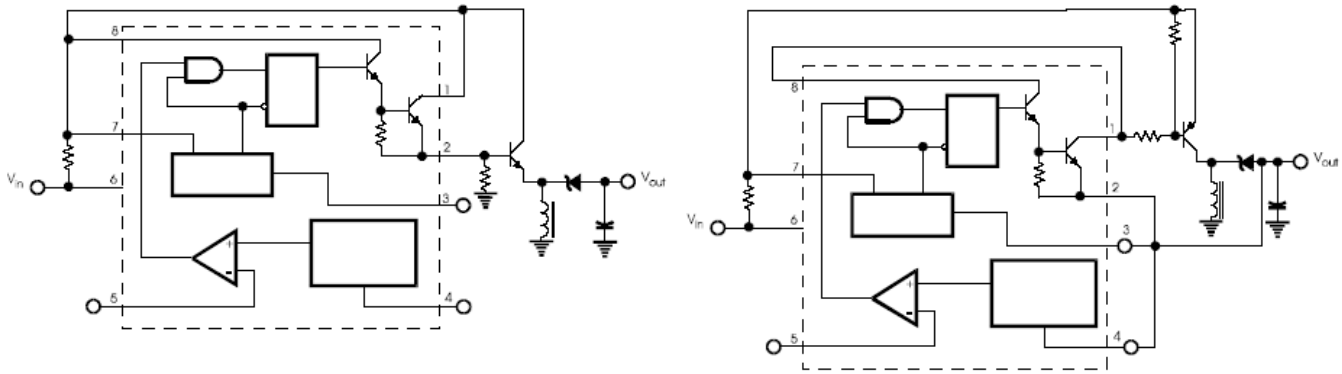


Figure 7. Design Formula Table

Calculation	Step-up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} + V_{sat}}$
$(t_{on}+t_{off})max$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4.0 \times 10^{-5}\ t_{on}$	$4.0 \times 10^{-5}\ t_{on}$	$4.0 \times 10^{-5}\ t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}\left[\frac{t_{on}}{t_{off}} + 1\right]$	$2I_{out(max)}$	$2I_{out(max)}\left[\frac{t_{on}}{t_{off}} + 1\right]$
R_{SC}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left[\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right] x\ t_{on(max)}$	$\left[\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right] x\ t_{on(max)}$	$\left[\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right] x\ t_{on(max)}$
C_O	$9\frac{I_{out}t_{on}}{V_{ripple(PP)}}$	$\frac{I_{pk(switch)}\ (t_{on} + t_{off})}{8V_{ripple(PP)}}$	$9\frac{I_{out}t_{on}}{V_{ripple(PP)}}$

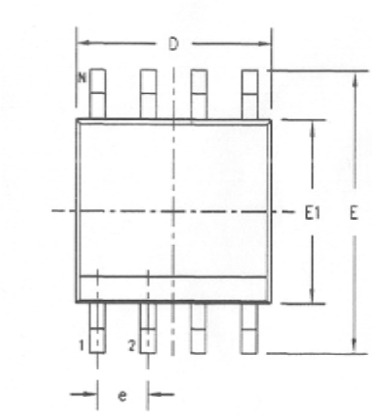
TERMS AND DEFINITIONS

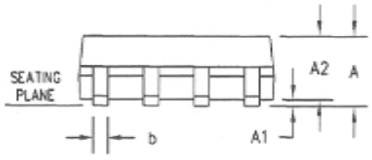
V_{sat} – Saturation voltage of the output switch.
V_F – Forward voltage drop of the output rectifier.
The following power supply characteristics must be chosen:

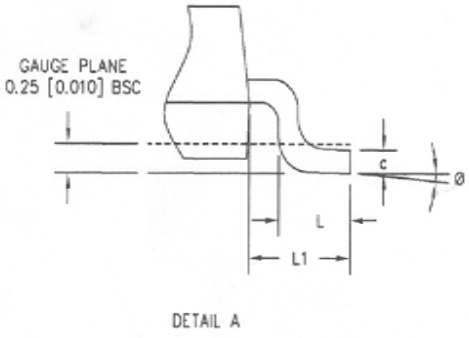
V_{in} – Nominal input voltage.
V_{out} – Desired output voltage, $\lvert V_{out}\rvert = 1.25\left[1 + \frac{R_2}{R_1}\right]$
I_{out} – Desired output current.
f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_O.
$V_{ripple(p-p)}$ – Desired peack-to-peack output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

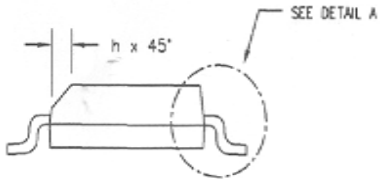
8L-SOIC PACKAGE DIMENSION

8-Lead SOIC Plastic
Surface Mounted Package
SLI Package Code: D8







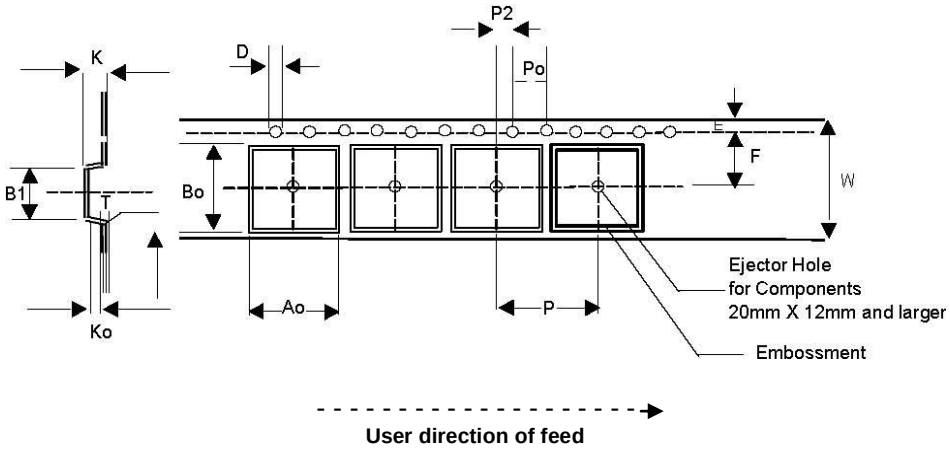


	DIMENSION IN INCHES			DIMENSION IN MM		
SYM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.059	0.062	0.065	1.50	1.57	1.65
A1	0.004	0.008	0.010	0.10	0.20	0.25
A2	0.051	0.054	0.057	1.30	1.37	1.45
b	0.013	0.016	0.020	0.33	0.41	0.51
c	0.007	0.008	0.010	0.18	0.20	0.25
D	0.191	0.193	0.195	4.85	4.90	4.95
E1	0.151	0.153	0.155	3.84	3.89	3.94
E	0.228	0.234	0.240	5.79	5.94	6.10
e		0.050			1.27	
L	0.020	0.024	0.032	0.51	0.61	0.81
L1	0.039	0.041	0.043	0.99	1.04	1.09
Ø	0*	-	B*	0*	-	B*
h	0.011	0.015	0.019	0.28	0.38	0.48

NOTES:
1. **DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.**
2. **COPLANARITY APPLIES TO THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.003" [0.08 mm].**
3. **BASED FROM JEDEC NS-012 VARIATION AA.**

PACKAGE MECHANICAL DRAWING

Surface Mountable Tape & Reel Specifications in mm (inch)
(SOIC)

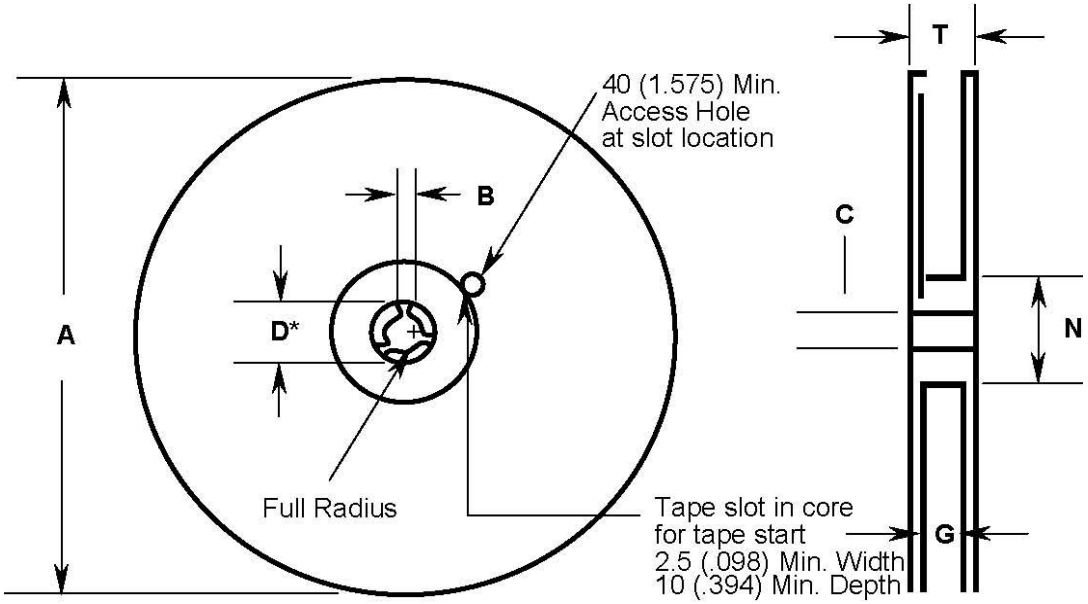


Tape Size (W)	D	E	P0	T (Max)	A0, B0, K0	T1 (Max)	Constant
8, 12, 16, 24mm	1.55±0.05 (.061±.002)	1.75±0.10 (.069±.004)	4.0±0.10 (.157±.004)	0.400 (.016)	See Note	0.100 (.004)	Dimensions

Tape Size (W)	B1 Max.	D1 Min.	F	K Max.	P2	
8 mm	4.2 (.165)	1.0 (.039)	3.5±0.05 (.138±.002)	2.4 (.094)	2.0±.05	
12 mm	8.2 (.323)	1.5 (.059)	5.5±0.05 (.217±.002)	4.5 (.177)	.079±.002	Variable Dimensions

Per Package Requirement					
Components		Tape Width (W) mm	Cavity Pitch (P) mm	Devices per Reel	
				7” Reel	13” Reel
SOIC	8L	12	8	-	2500

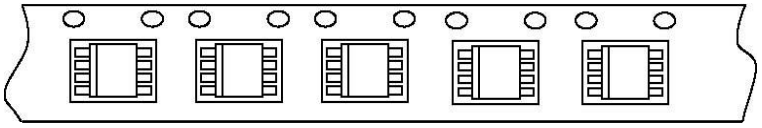
Note: Ao Bo Ko are determined by component size. The clearance between the component and the cavity must be within 0.05 [.002] min. to 0.50 [.020] max. for 8mm tape, 0.05 [.002] min to 0.65 [.026] max for 12mm tape.



REEL DIMENSIONS							
Tape Size	A Max.	B Min.	C	D* Min.	N Min.	G	T Max.
8mm	330 (12.992)	1.5 (.059)	13.0±0.20 (.152±.008)	20.2 (.795)	50 (1.973)	8.4±1.5 0.0 (.331±.059) 0.0	14.4 (.567)
12mm	330 (12.992)	1.5 (.059)	13.0±0.20 (.152±.008)	20.2 (.795)	50 (1.973)	12.4±2.0 0.0 (.488±.078) 0.0	14.4 (.567)

MECHANICAL POLARIZATION

SOIC-8L DEVICE



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