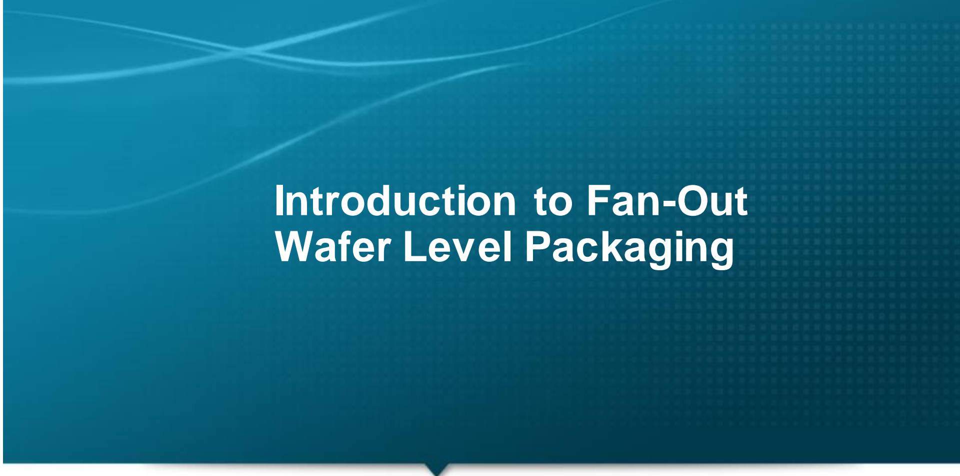
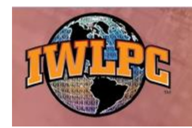




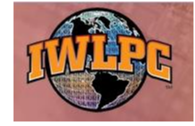
Beth Keser
Qualcomm Technologies, Inc.

IW LPC 2015– San Jose, CA, USA

October 15, 2015

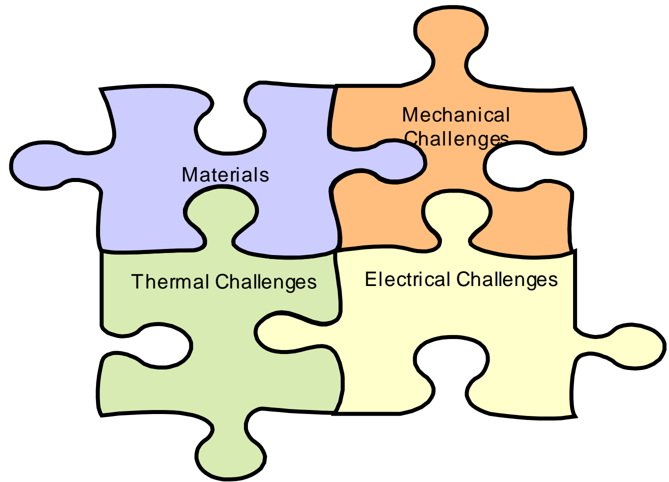
Outline

- Current Challenges in Packaging
- FOWLP Definitions and Advantages
- Process
- Applications
- Package Structures
- Material Challenges
- Equipment Challenges
- Die Drift
- Design Rules
- Reliability
- Roadmaps
- Panel
- Benchmarking

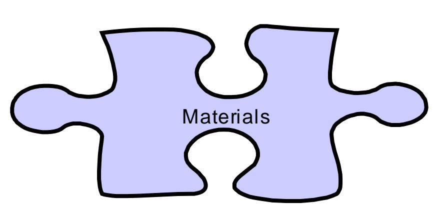


IW LPC 2015– San Jose, CA, USA October 15, 2015

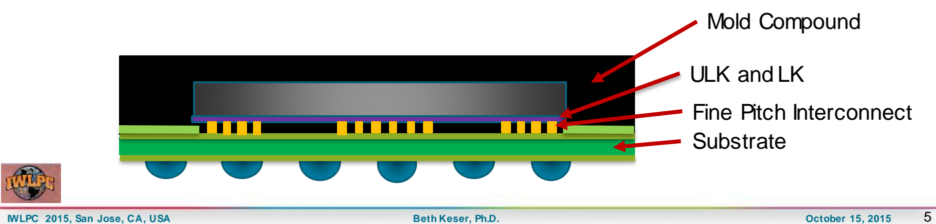
Technical Challenges of Packaging



Technical Challenges of Packaging

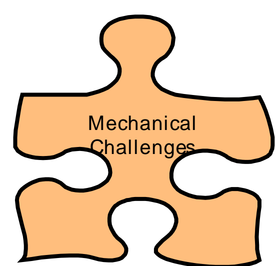


- Low K and Extreme Low K (dielectric constant) Dielectrics
- Fine Pitch Interconnects (<100μm)
- Low CTE, High Modulus Substrate Materials
- High CTE Mold Materials

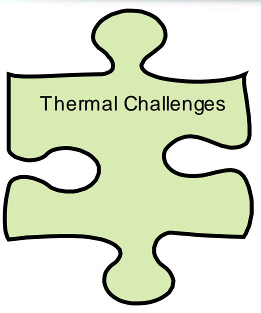


Technical Challenges of Packaging

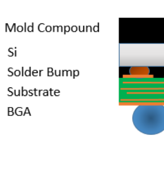
- Ultra thin die (<150μm)
- CTE Mismatch
- Warpage Control
- Preserving Si Strain Engineering

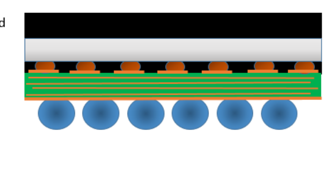


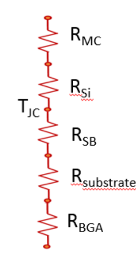
Technical Challenges of Packaging



- Higher Tj (>100°C)
- Poor thermal paths
- No air flow, closed system
- 3D Integration

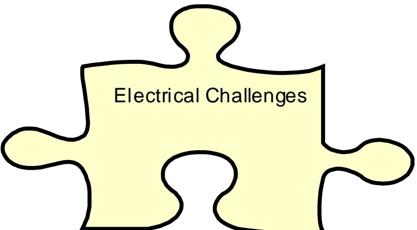




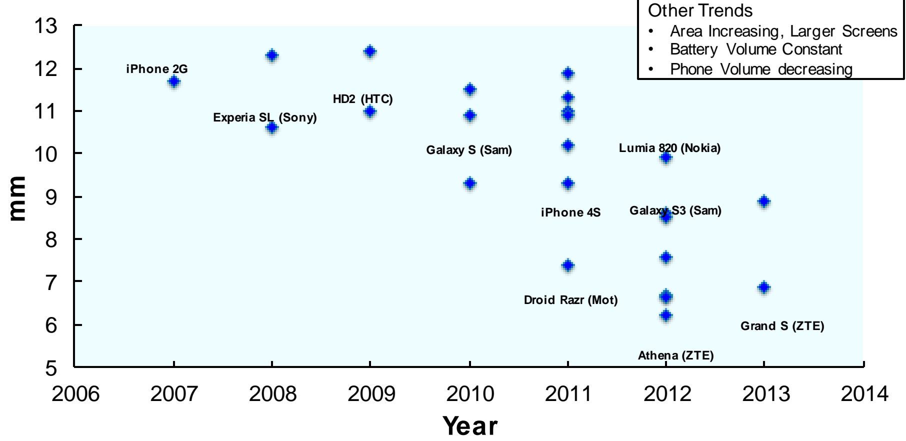


Technical Challenges of Packaging

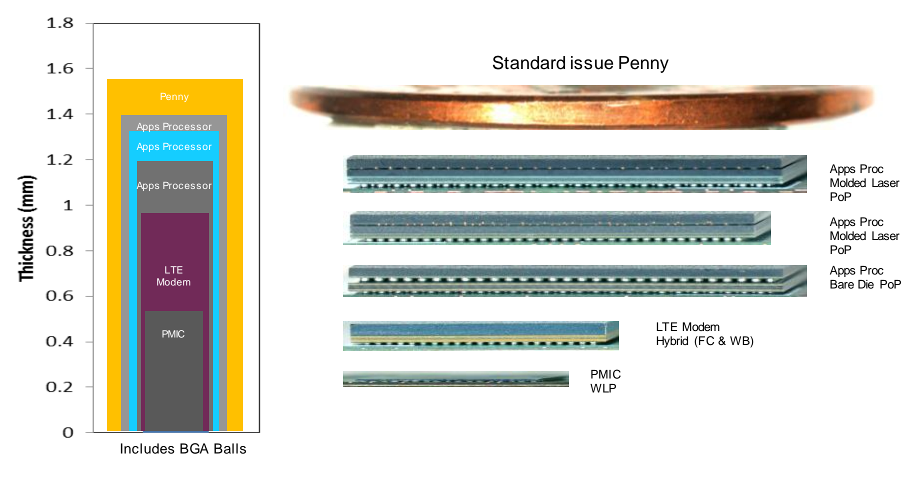
- Signal Integrity
- Power Distribution
- Functional Partitioning



Decrease in Handset Thickness Over Time



Height Comparison of Mobile Packages



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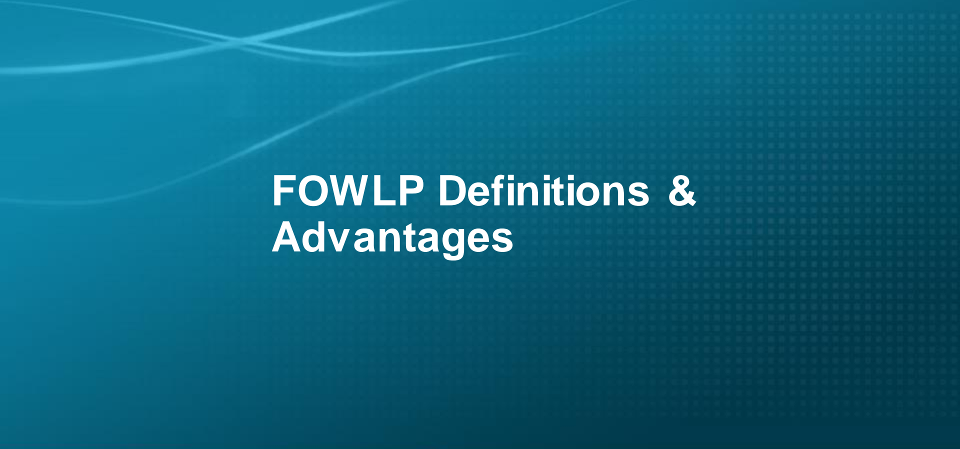

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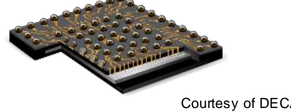
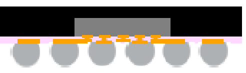
Definition

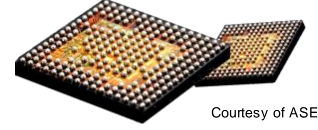
- Embedding known good die (KGD) into mold compound or substrate
- Building up interconnect layers from die to BGA balls on mold compound or substrate

"Fan-out WLP or FOWLP"
"Chips First"
"extended Wafer Level BGA or eWLB"
"Redistributed Chip Package or RCP"
"M-Series"
"Integrated Fan-Out"



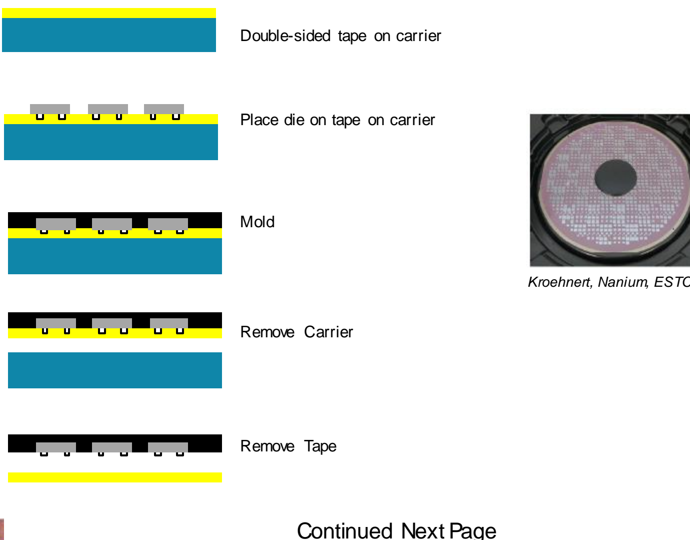
Courtesy of DECA





Courtesy of ASE

Typical FOWLP Process Flow



Kroehnert, Nanium, ESTC 2012

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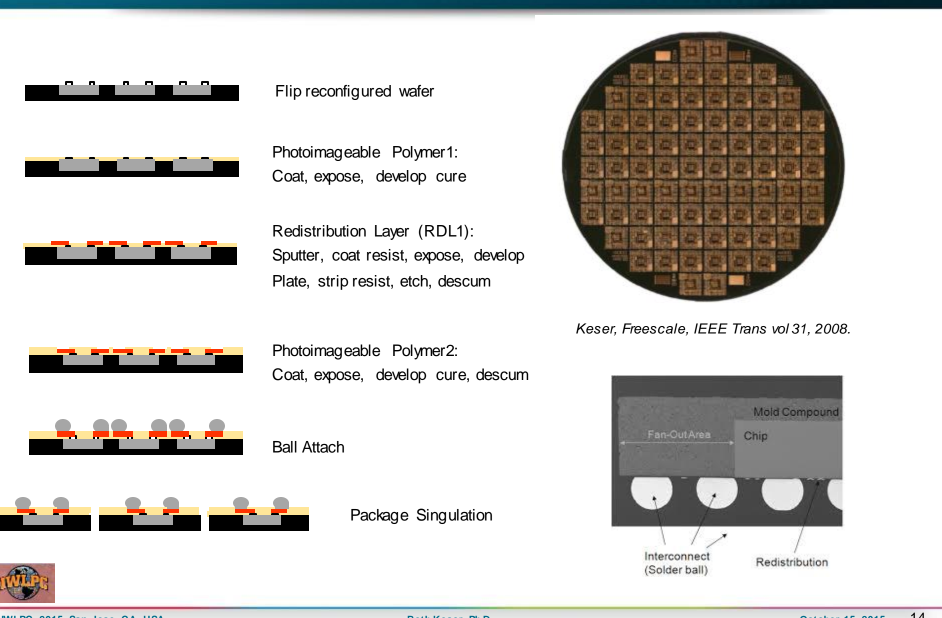
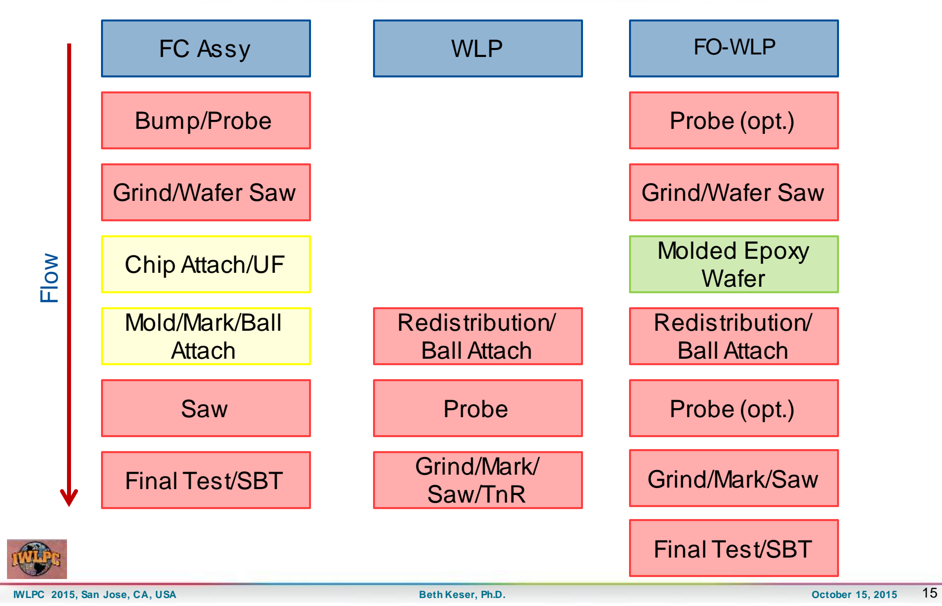
Typical FOWLP Process Flow



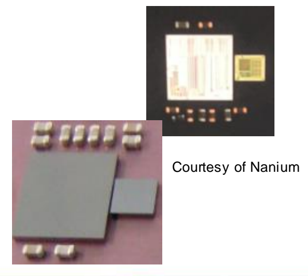
Keser, Freescale, IEEE Trans vol 31, 2008.

Packaging Process Flow Comparison



FOWLP Advantages

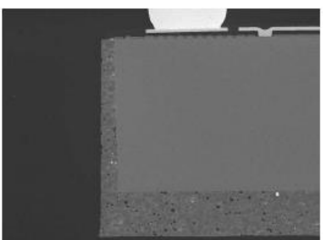
- Eliminates die interconnect (bump and wirebonds) and substrate
  - Excellent Electrical Performance
    - Shorter interconnects = Lower parasitics
  - Eliminate interconnect stress and ELK (extreme low dielectric constant) crack delamination issues
- Fine Line/Space (L/S) for better routability
- Finer pad pitch on die than flip chip
- Thin package, Smaller Form Factor
- Potential SiP, Multi-die, 3D Solution
  - High integration
    - Heterogeneous chips + passives



Courtesy of Nanium

FOWLP Advantages Compared to WLP

- More real estate for pins than WLP
- Batch packaging process like WLP, but with KGD
  - Probe of bare pad on wafer needs to be enabled
- Enables final test
- Mold compound to protect die sidewalls from chipping/cracking during SMT



Mold compound sidewall can be as thin as 50µm creating “eWLCSP”
Strothmann, ECTC, 2014

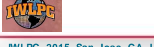
3D FOWLP Advantages

- Eliminates warpage and coplanarity issues
- PoP Height reduction
- Eliminates stress on die from Pb-free bump
- Thicker die allowed

Courtesy of ASE

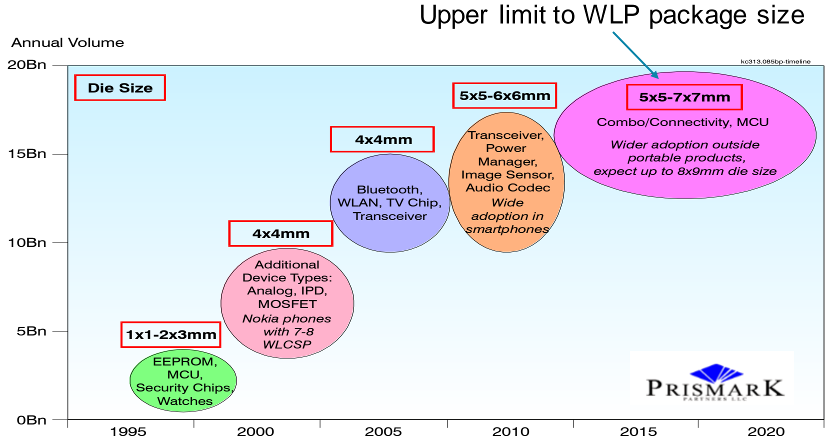
FOWLP Disadvantages

- Capacity
- Yield
- Probe of bare die for KGD needs to be enabled
- Chips First
  - Committing chip to package
  - Other packaging uses KGD with Known Good Substrate
- Design not flexible
  - Design for FOWLP to take advantage of short interconnects
  - Cannot be re-used in WB or FC part without redesign

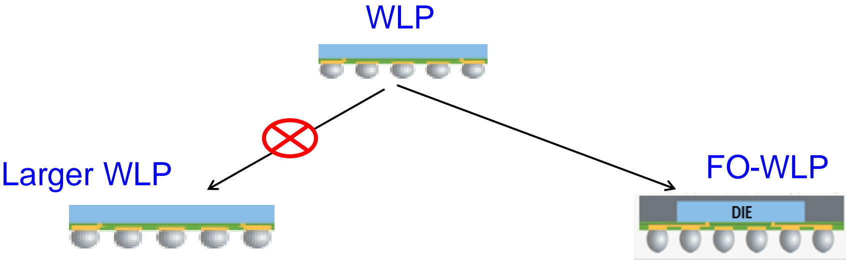


FOWLP Applications

Wafer Level Packaging

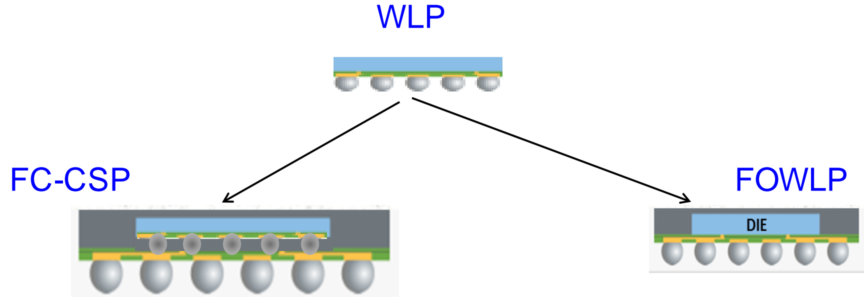


Applications: Enables Larger WLP



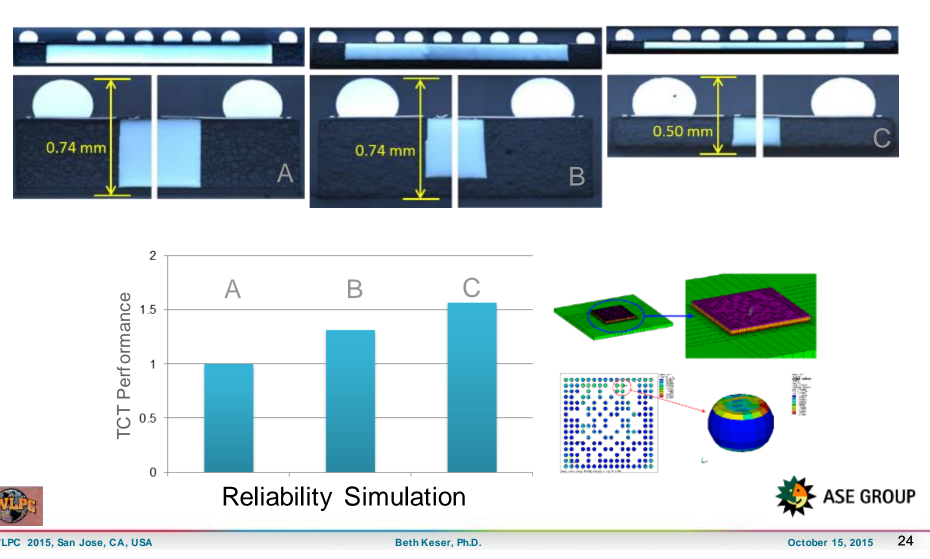
- FOWLP enables fan-out of high IO wafer level packages
- Better board level reliability
- No increase in Si area to accommodate IO
- FOWLP could potentially decrease Si area

Applications: Coarser Pitch WLP



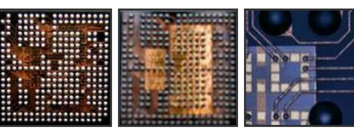
- Repackage WLP for applications that require coarser pitch
- Fast to market WLP with coarser pitch
- Fan-out offers smaller package size and lower cost

Applications: Thin Package

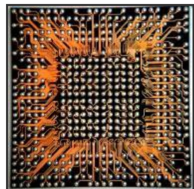


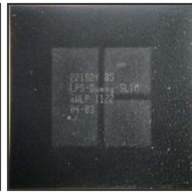
Applications: Multi-die Module

- **Modules with smaller footprint**
  - Minimizing spacing between die and die to package edge.

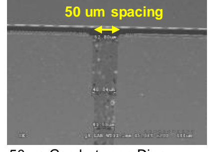


8X8 2-Die Test vehicle (Qualified)

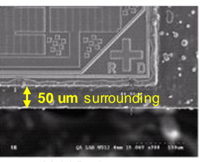




13X13 3-Die Test vehicle (CLR passed)



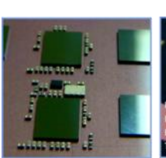
50µm Gap between Dies

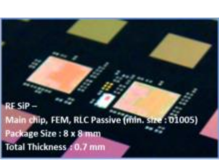


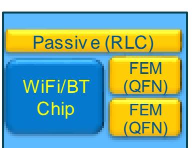
50µm Mold Perimeter

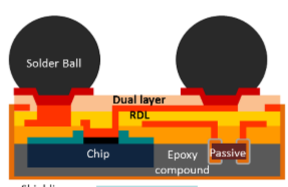
Application: Multi-Component RF Modules

- Integrated chips & passives for front-end module (FEM).
  - Multi-die and passive integration
  - Multi-layer redistribution layer (RDL) allows interconnection
  - Inductors in RDL
  - Sputtered or plated shielding





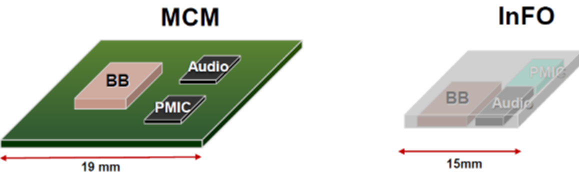




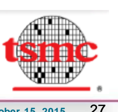
ASE GROUP

Applications: SiP Package Shrink

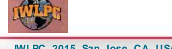
- 15x15 multi-die FOWLP enables products that demand higher pin count (up to 1000) and higher integration
  - e.g. baseband module
- Reduces baseband module form factor by 55% in thickness and 40% in package area



Example: Baseband module with 700 I/Os at 0.4mm ball pitch

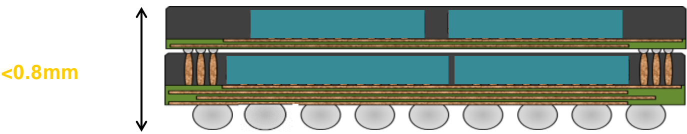


InFO = Integrated Fan Out



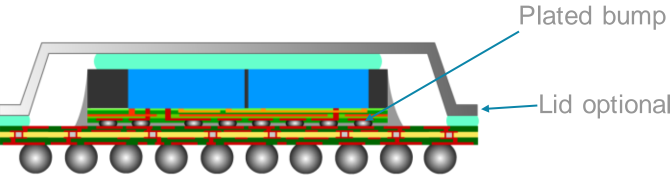
Applications: Package on Package

- Eliminates warpage and coplanarity issues
  - No substrate
- PoP Height reduction
- Eliminates stress on die from bump interconnect



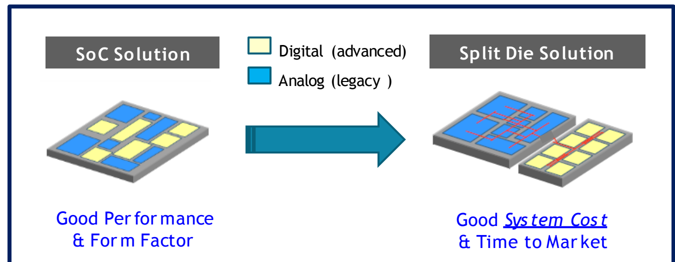
Application: High Density Die-to-Die (D2D)

- Fan-out on substrate
- Mobile phone/Tablet, AP/Baseband + RF/Analog, PMIC, Low-end CPUs, GPUs
  - Shorter die-to-die (D2D) connect for good electrical performance
  - High IO (input/output)
  - Fine L/S (2/2)
  - No interposer lowers cost



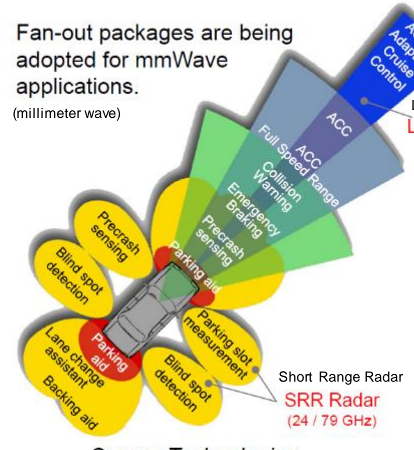
Applications: Split die

- For next generation application processor
  - Split analog and digital portions of die into 2 die nodes (e.g. 16nm/10nm)
  - Create die to die connections (D2D) in FOWLP package
- Benefit
  - Lowers cost
    - Development
    - Wafer cost
  - Higher fab yields
  - Faster time to market



Application: Automotive

Fan-out packages are being adopted for mmWave applications.
(millimeter wave)

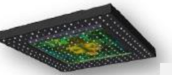


Sensor Technologies for Driver Assistance Systems

77GHz Radar System

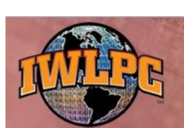
Redistributed Chip Package (RCP)

- Dramatic **volumetric shrink** of current and future systems: **40-90%.**
- Increased functionality via **heterogeneous integration**.
- Improvement in **system performance** (low parasitics, low inductance).
- Improved **board level reliability**.

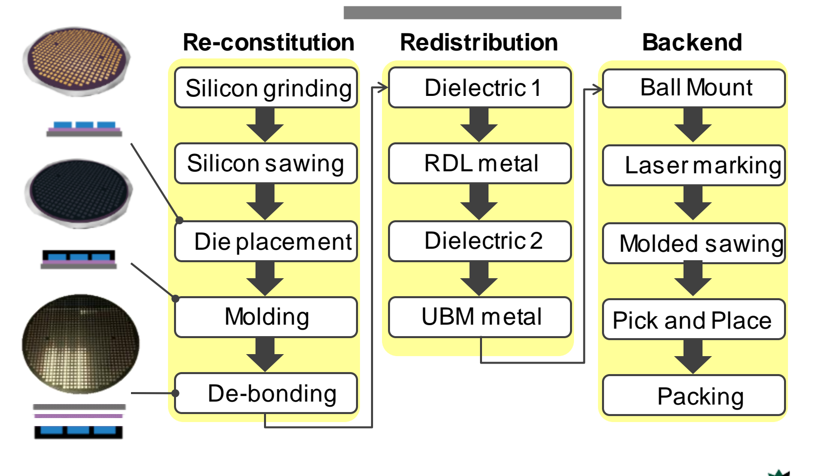


Daves, SemiconWest, 2014

Fan-Out and Embedded Technologies (Package Structures)



eWLB Process Flow



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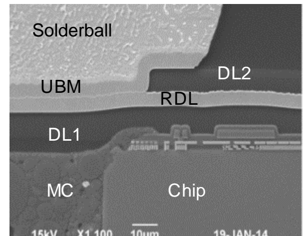
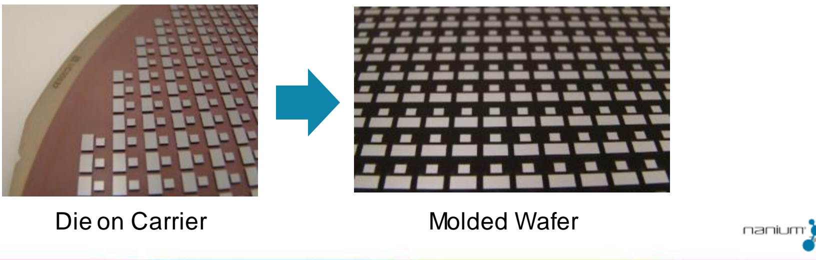
eWLB Licensees

- STATSChipPAC
- Nanium
- ASE
- IFX also has eWLB internal manufacturing capability on 200mm line in Germany

Nanium Product Examples

- Multi-Die eWLB with 2 die in High Volume Manufacturing (HVM)
  - 6.3 x 4.7 mm² package size
  - 130 IOs, 0.4 pitch
  - No underfill required
  - 1L-Cu-RDL
  - L/S 10/10
  - Cu UBM





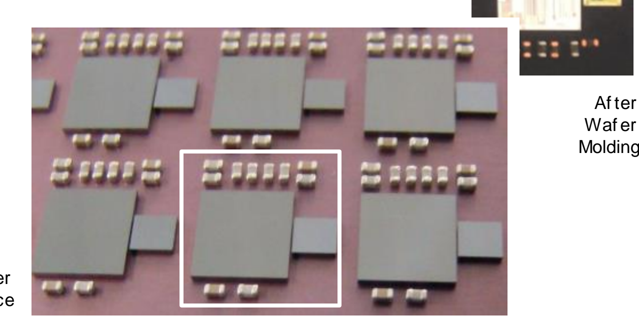
Die on Carrier

Molded Wafer

Nanium Product Examples

- Active and Passive Integration in eWLB
  - 8.7 x 7.9 mm² package size
  - WLSIP with 2 active die
    10 passives (0201)
  - 2L-RDL

After
Wafer
Molding

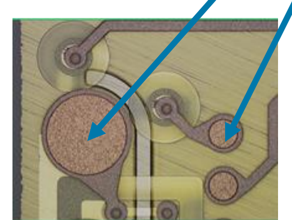


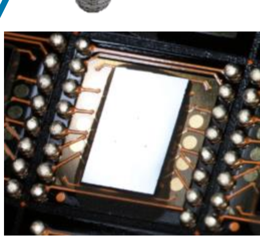
After
Pick&Place

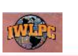
Nanium Product Examples

- Thin 3D Face-to-Face Bonded eWLB Package
  - Package size = 16mm²
  - Package Height < 0.8mm
  - 0.5 pitch
  - bump 200um pitch
  - Flip chip assy on eWLB Wafer after RDL
  - Reduced Chip-to-Chip vertical interconnection.

BGA FC

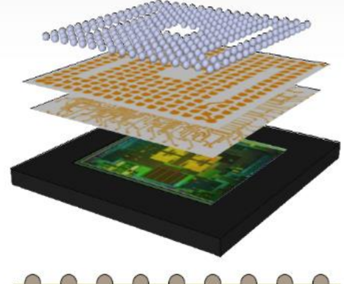




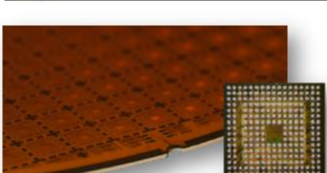


Freescale's Redistributed Chip Package (RCP)

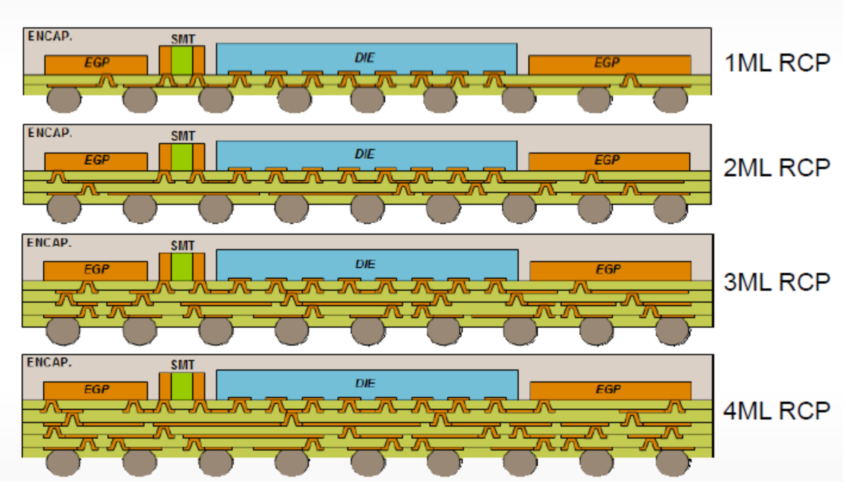
- Freescale proprietary technology
- Scalable, fan-out chip scale package
- A technology solution for:
  - Small form factor packages
  - High performance
  - Multi-die, heterogeneous integration
- 2D, 3D System in Package (SiP) solution
- Key applications
  - Medical
  - Defense
  - Migrate to consumer, industrial and auto



Mold Compound DIE

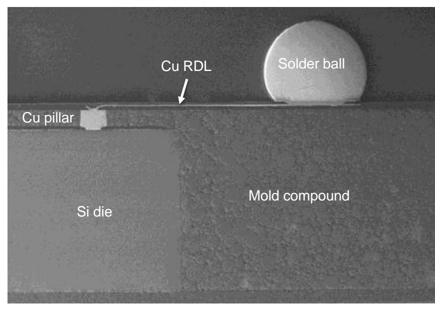


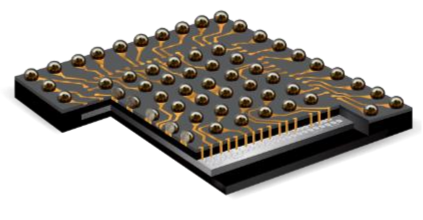
Freescale's Redistributed Chip Package (RCP)



EGP = Embedded Ground Plane

DECA Technologies' M-Series

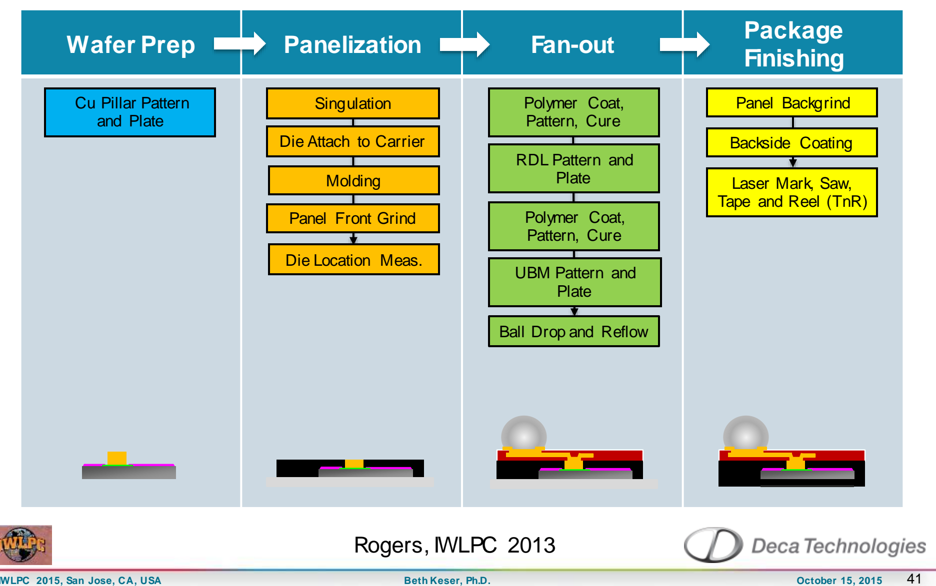




- Die encased in mold compound
- Cu bump interconnect to fan-out structure
- Adaptive Patterning™ to address die shift
- Solar-based processes and equipment

Deca Technologies

DECA's M-Series Process Flow

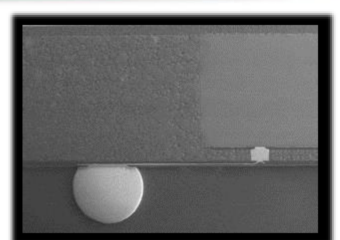


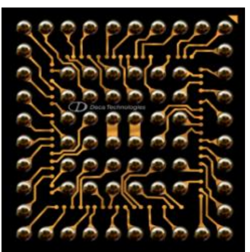
Rogers, IWLPC 2013

Deca Technologies

DECA's M-Series with Adaptive Patterning

- Rugged fan-out package with fully encapsulated option
- Planar patterning surface to enable advanced geometries
- Improved reliability for larger silicon devices
- Adaptive patterning to enable high yields on fine pitch bond pads
- Capable across wide range of IC device types
- Low cost with high speed die attach and solar wafer fab inspired Autoline



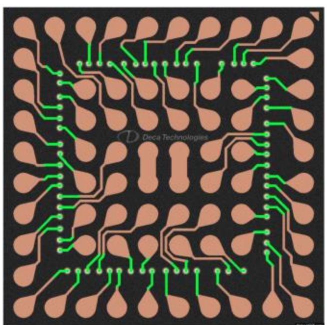


Scanlan, IWLPC, 2012

DECA's Adaptive Patterning Methods

Adaptive Routing

- Dynamically adapt RDL routing to accurately align to true die position

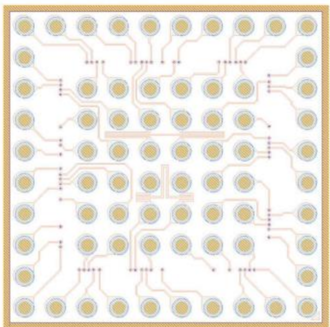


- BGA array fixed to package outline
- Enables multi-die fan-out

Scanlan, IWLPC, 2012

Adaptive Alignment

- Align the entire RDL layer to true die position within the unit

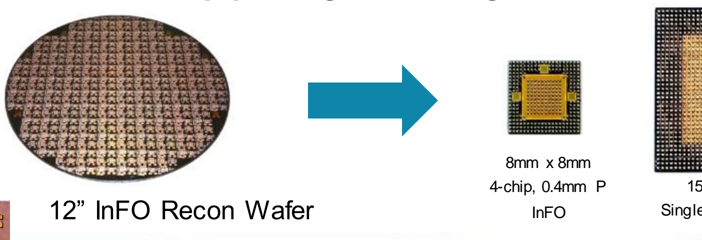


- Enables high metal density designs
- Precise alignment of inductors to die

Deca Technologies

TSMC's Integrated Fan-Out (InFO)

- Ultra fine pitch RDL (L/S down to ***2/2um***)
- 15mm x 15mm package size for single die
- 8mm x 8mm package size with 4 chips
- Ultra-high Q (~60) built in inductor
- Ultra-thin (0.45mm) package
- Supports PoP
- ***Seamless chip-package co-design***

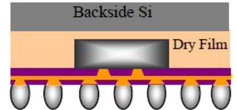


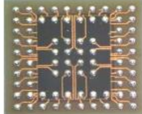
12" InFO Recon Wafer

8mm x 8mm 4-chip, 0.4mm P InFO

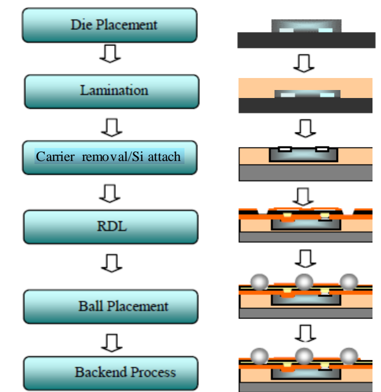
15mm x 15mm Single-chip, 0.4mm P InFO

SPIL's Single Die Fan-Out (SDFO)





- Dry film lamination encapsulant
  - Requires thin die (50um)
- Si carrier becomes part of package
  - Reduces warpage (empirical and simulation)
  - Improved solder joint life (TC and Drop) (simulation only)
  - Passed thermal cycles on board (TCoB) and Package level rel



Hsu, ECTC, 2012

SPIL's Single Die Fan-Out (SDFO)

SPIL Test Vehicle

Backside Silicon
Die
RDL

Backside Silicon 340 um
Encapsulation Die 50um Trace

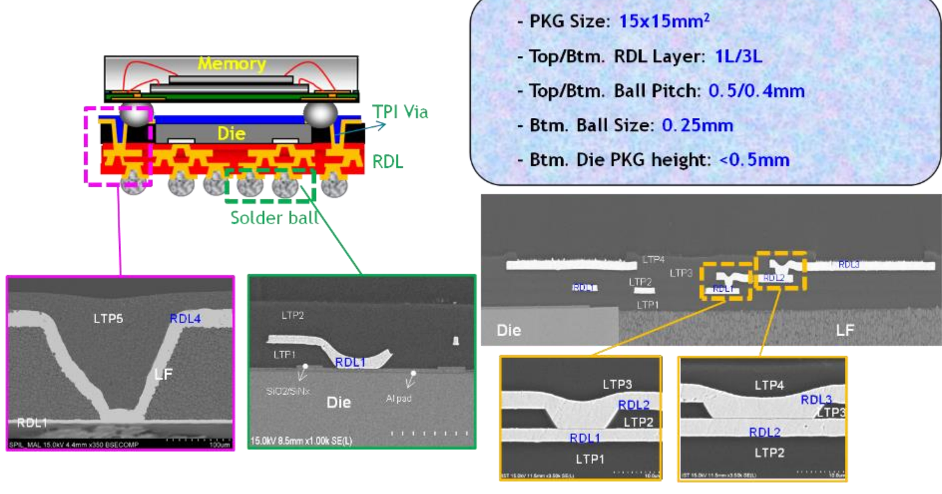
Encapsulation 80 um

Bump Pad
RDL 190 um LTP

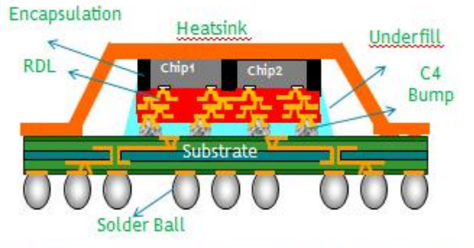
LTP = Low Temperature Cure Polymer

SPIL

SPIL's Through Package Interconnection Fan-out (TPI-FO)



SPIL's Multi-Chip Module Fan-Out (MCM-FO)

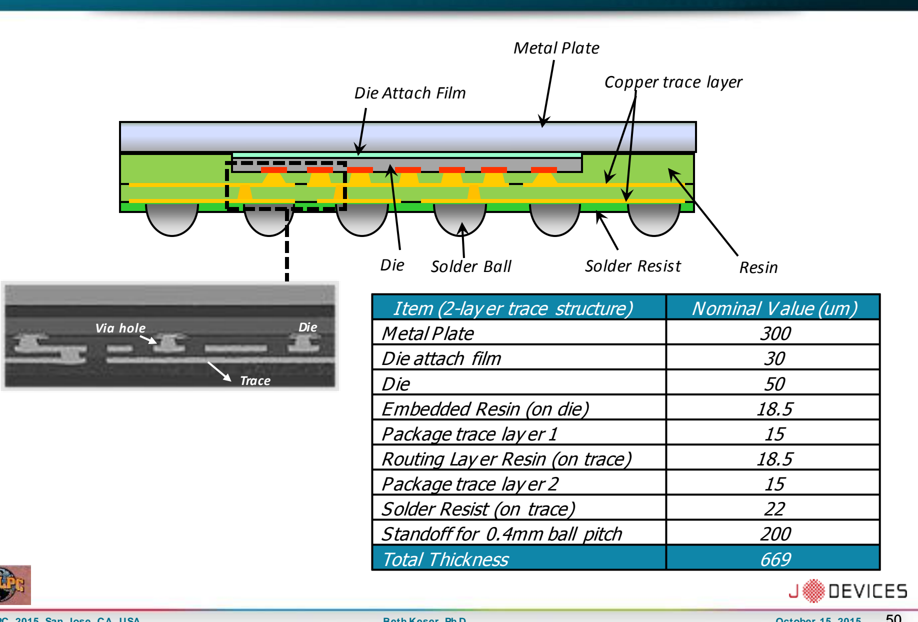


- PKG Size: BGA 45x45mm²
- Die-to-Die Gap: 80um
- RDL layer : 3L
- BGA ball pitch/size: 1.0/0.6mm

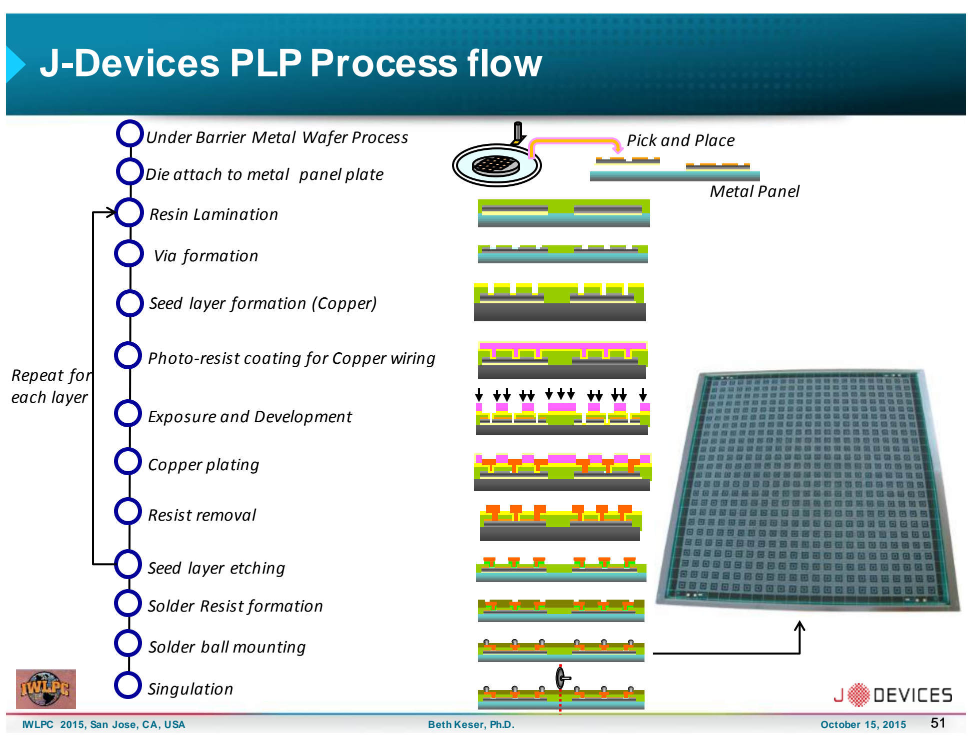
Embedded Die in Panel

- Applications
  - Low IO count devices
    - uDCDC, Audio, Power Management, Charging, Envelope Tracking
- Challenges
  - Supply Chain
  - Standardization
  - Volume to drive low cost
  - Coarse L/S

J-Devices Panel Level Package (PLP)



Item (2-layer trace structure)	Nominal Value (um)
Metal Plate	300
Die attach film	30
Die	50
Embedded Resin (on die)	18.5
Package trace layer 1	15
Routing Layer Resin (on trace)	18.5
Package trace layer 2	15
Solder Resist (on trace)	22
Standoff for 0.4mm ball pitch	200
Total Thickness	669


J-Devices PLP Process flow
Under Barrier Metal Wafer Process
Die attach to metal panel plate
Resin Lamination
Via formation
Seed layer formation (Copper)
Photo-resist coating for Copper wiring
Exposure and Development
Copper plating
Resist removal
Seed layer etching
Solder Resist formation
Solder ball mounting
Singulation
Repeat for each layer
Pick and Place
Metal Panel
J DEVICES
IWLPC 2015, San Jose, CA, USA
Beth Keser, Ph.D.
October 15, 2015
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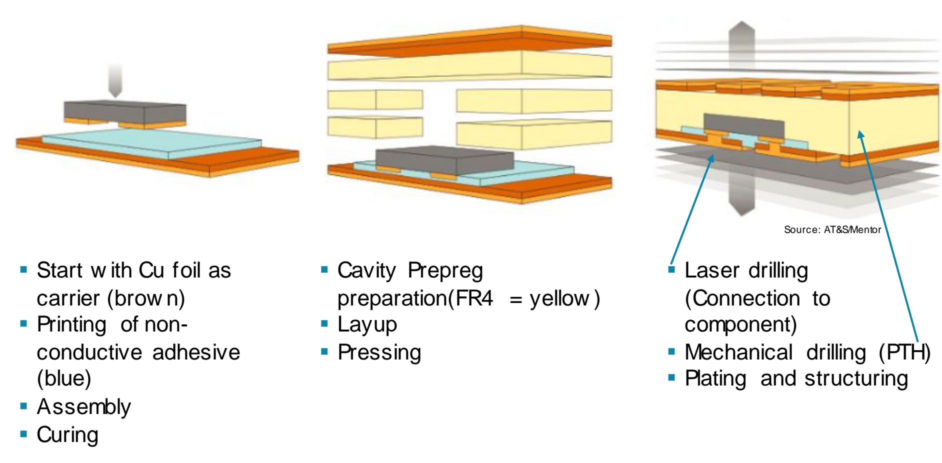
AT&S Embedded Component Package (ECP®) Process Flow
Source: AT&S/Mentor
Start with Cu foil as carrier (brown)
Printing of non-conductive adhesive (blue)
Assembly
Curing
Cavity Prepreg preparation(FR4 = yellow)
Layup
Pressing
Laser drilling (Connection to component)
Mechanical drilling (PTH)
Plating and structuring

Structuring can be done by semi additive or subtractive process
24”
AT&S
IWLPC 2015, San Jose, CA, USA
Beth Keser, Ph.D.
October 15, 2015
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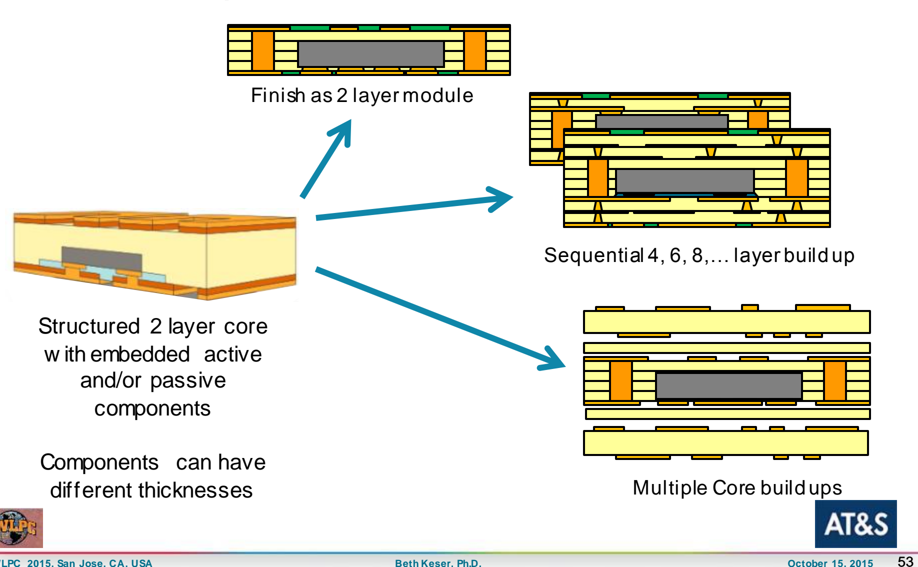
AT&S Embedded Component Package (ECP®)
ECP® Stack ups
Finish as 2 layer module
Sequential 4, 6, 8,… layer build up
Structured 2 layer core with embedded active and/or passive components
Components can have different thicknesses
Multiple Core build ups
AT&S
IWLPC 2015, San Jose, CA, USA
Beth Keser, Ph.D.
October 15, 2015
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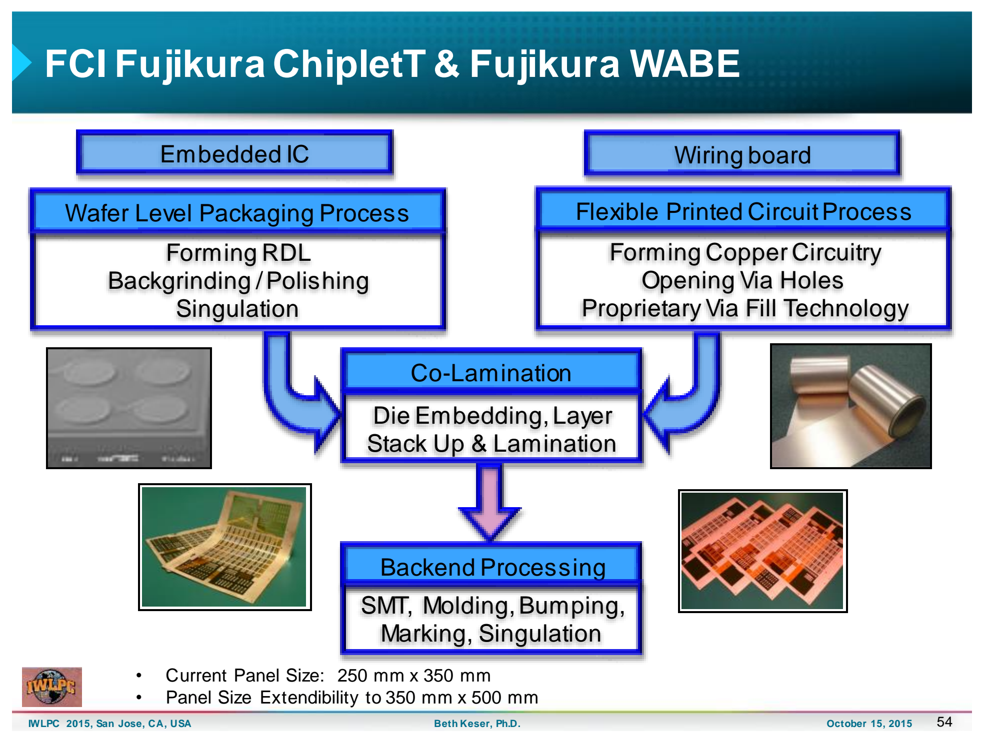
FCI Fujikura ChipletT & Fujikura WABE
Embedded IC
Wiring board
Wafer Level Packaging Process
Forming RDL
Backgrinding / Polishing
Singulation
Flexible Printed Circuit Process
Forming Copper Circuitry
Opening Via Holes
Proprietary Via Fill Technology
Co-Lamination
Die Embedding, Layer Stack Up & Lamination
Backend Processing
SMT, Molding, Bumping, Marking, Singulation
Current Panel Size: 250 mm x 350 mm
Panel Size Extendibility to 350 mm x 500 mm
IWLPC 2015, San Jose, CA, USA
Beth Keser, Ph.D.
October 15, 2015
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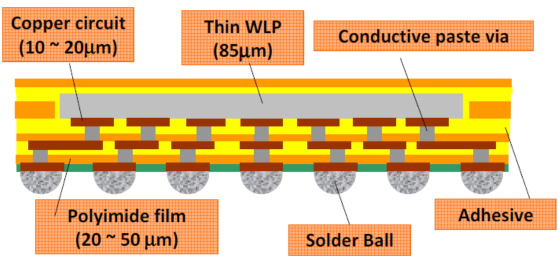
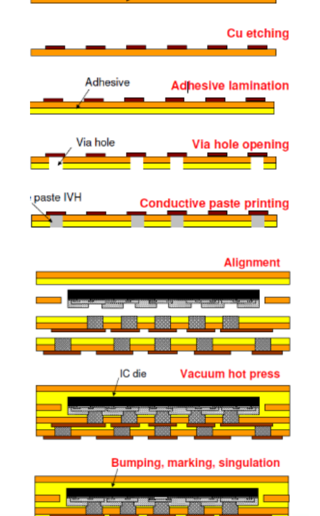
Fujikura Wafer And Board level device Embedded package (WABE)

- Based on flexible, not rigid, board technology
  - Roll to roll process
  - Semi-additive plated Cu 20/20 L/S





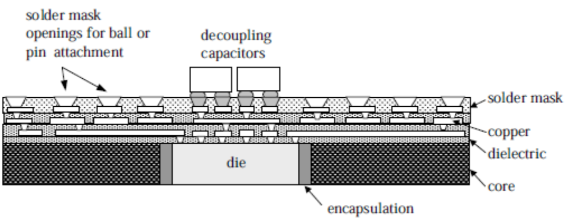
(1) Ultrathin WLP
(2) Flex based multilayer wiring board
(3) Interstitial Via Hole filled by Conductive paste

Okude, Semicon West, 2012

Other Technologies

- Intel's Bumpless Build-up Layer (BBUL)
  - Embedded die

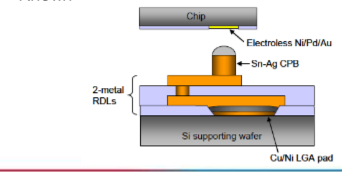
Tow le, Proc. ASME Int. Mech. Eng. Congress and Exposition, 2001

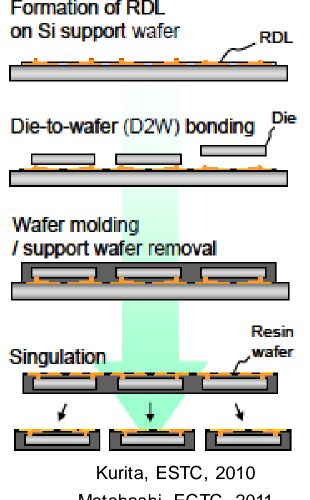


  - Die embedded in a substrate, such as bismaleimide triazine (BT) laminate or a copper heat spreader
  - Encapsulation of the die in substrate done w ith dispensed encapsulation material
  - One or more build-up layers laminated on top
  - Build-up layers are made w ith a standard high-density integration (HDI) patterning technology
    - Build-up is similar to what is ty pically used f or advanced organic packages and printed circuit boards
    - Dielectric is dry f ilm Ajinomoto ABF
    - Standard microv ia f ormation process, such as laser drilling, makes the connections between the build-up lay ers and the die bond pads

Other Technologies

- Renesas SiWLP (System in Wafer Level Package)
  - "RDL First"
- Process
  - PI1 layer
  - Eplated Cu/Ni filled metal vias for external terminals
  - Cu plated RDL
  - PI2 layer
  - Cu plated SnAg capped pillars
  - Chip pads required e'less Ni/Pd/Au
  - Chip attach to RDL wafer
  - Reflow
  - Mold and underfill simultaneously
- Advantages
  - No die drift allows for finer pitch I/O pads on chip
  - No low cure dielectric required
  - Known good RDL (probe Cu pillars on RDL wafer)



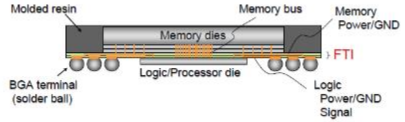


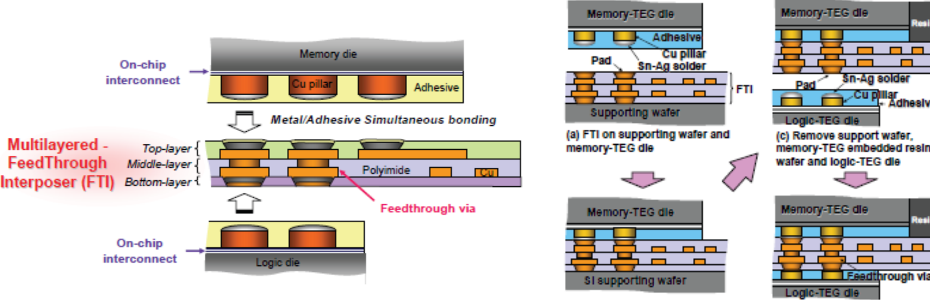
Kurita, ESTC, 2010

Motohashi, ECTC, 2011

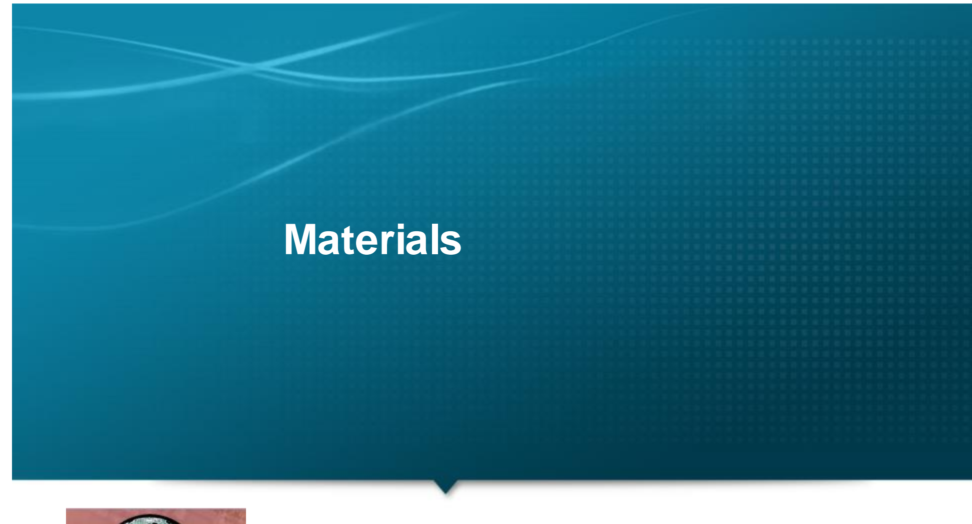
Other Technologies

- Renesas (formerly NEC) SMAFTI (SMArt chip connection with Feed Through Interposer)





Motohashi, ECTC, 2009



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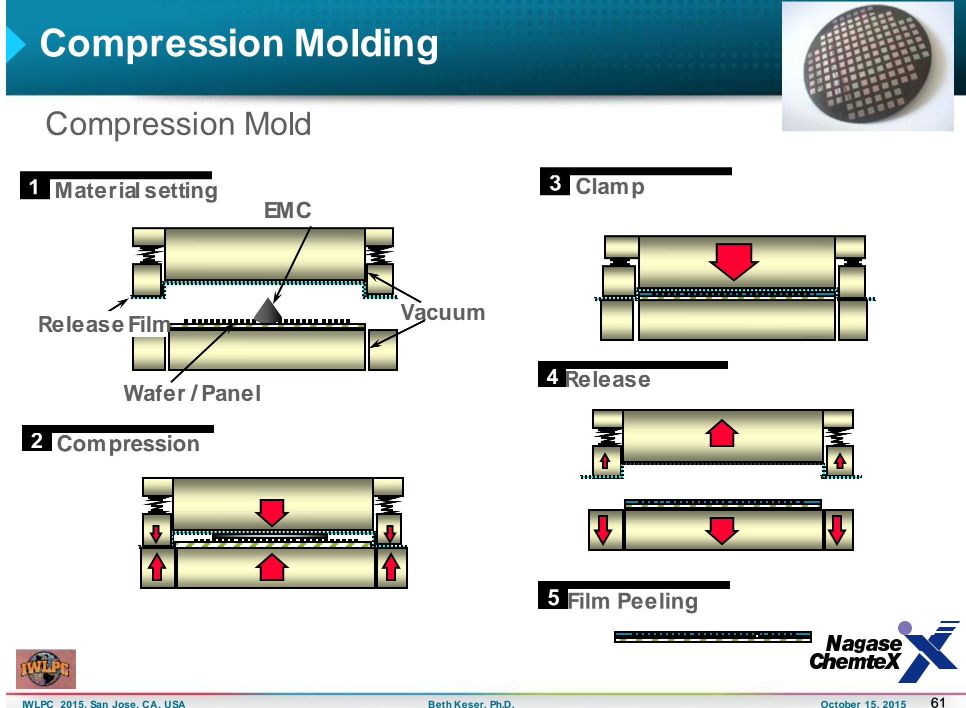
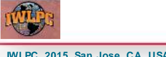
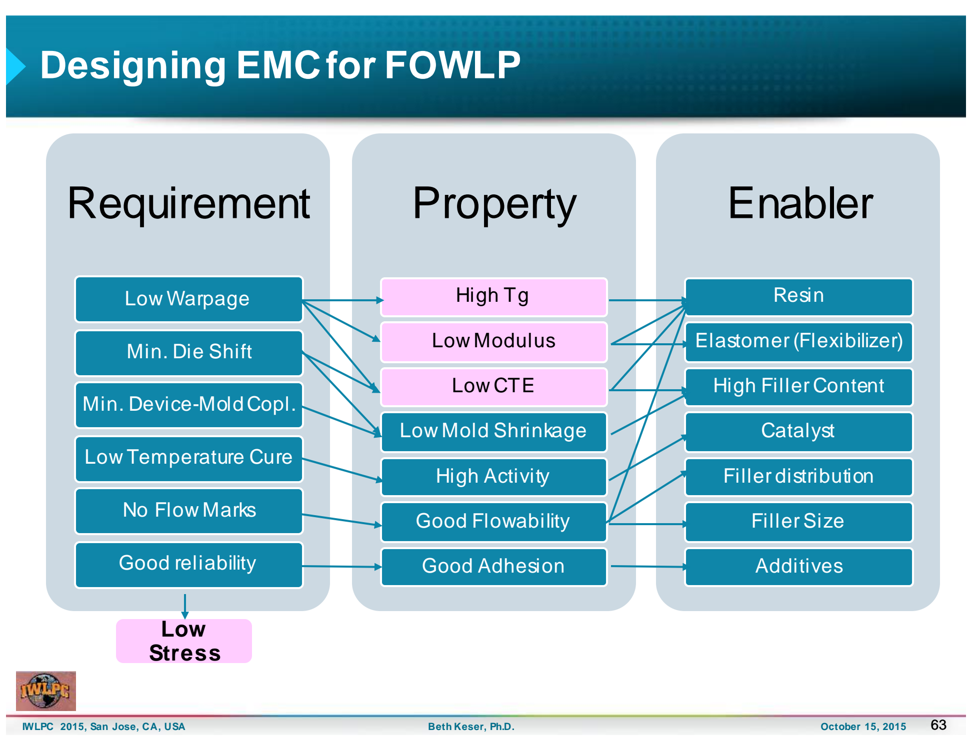
October 15, 2015



Epoxy Mold Compound Challenges for FOWLP

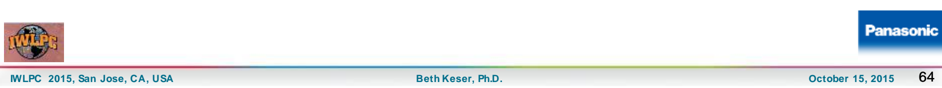
- Cost
- Low temperature cure
  - Lower than release temperature of debond tape
- Cure Time/Cycle Time
  - Short time in mold required
- Die drift
  - Minimal cure shrinkage
- Warpage
- Flow Marks/Fill





EMC Challenges

Challenge		Warpage	Flow mark	Flow ability
Carrier size	Bigger	Bigger	Worse	Worse
	Smaller	Smaller	Better	Better
Mold thickness	Thicker	Bigger	Better	Better
	Thinner	Smaller	Worse	Worse

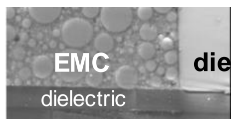


EMC Challenges

- Liquid vs. Solid EMC

Type	Cost	Viscosity	Handling	Cure Shrinkage	Floor/Shelf Life
Liquid	+	+++	+++	+	+
Solid	++	+	++	+++	+++

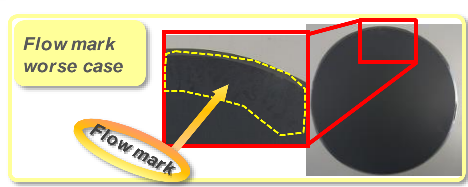
- Liquid
  - Good flowability/viscosity → Less voids, better fill, less flow marks
  - Better handling → No particles
- Solid
  - Less Cure shrinkage → Better stand off, less die drift

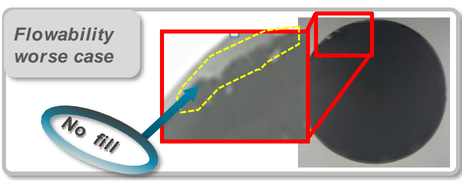


courtesy of Hitachi

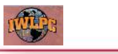
courtesy of Sumitomo

EMC Challenges



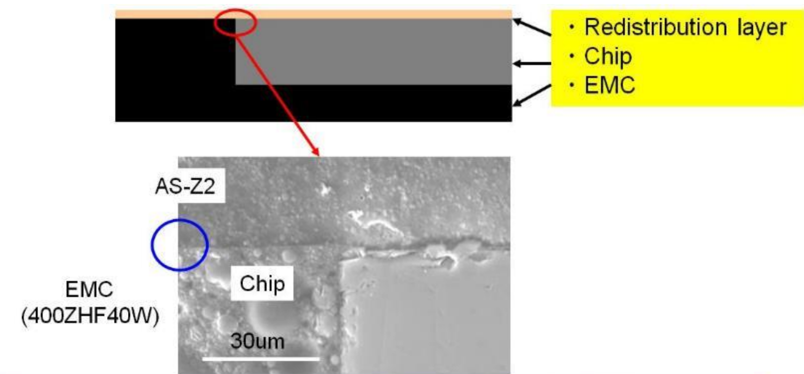


Panasonic



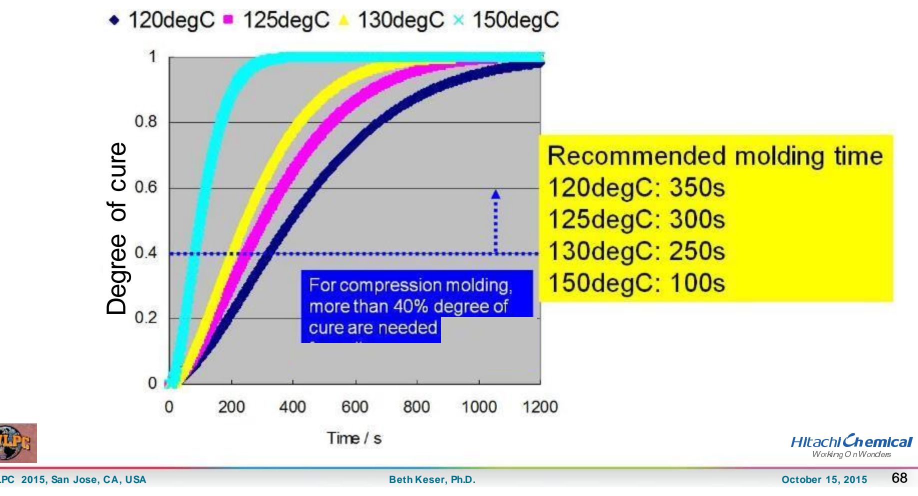
Material Characteristics

Results of die-stand off

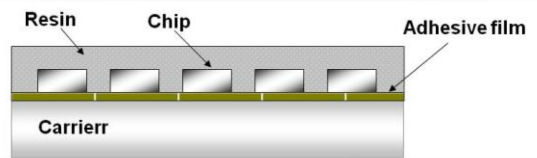


Time in Mold

- Gel time is the time required for a thermosetting mold compound to effectively solidify at the molding temperature
- Gel time must be reached in mold before transfer to PMC

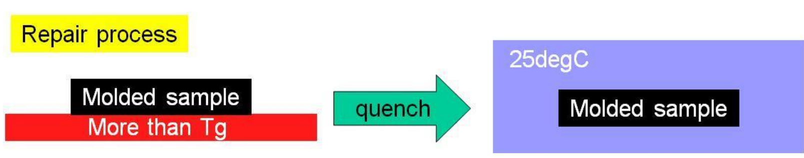


Hitachi TV



Item		Condition
Chip	Size	7x7x0.4mm
	Number of amount	400
PKG	Size	8x8x0.5mm
Adhesive film	Thickness	100um
Carrier	Diameter	8 inch
	Thickness	2mm
Molding condition	Mold size	200mm
	Thickness	0.5mm
	Clamping force	100kN
	Temp. & Time	125degC/300sec
	Post Mold Cure	150degC/1hr

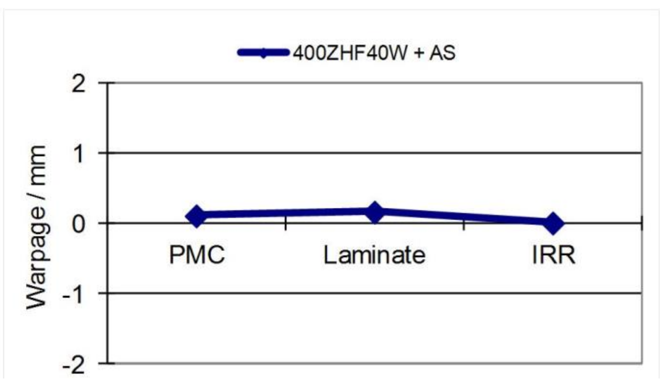
Warpage Relaxation ("Repair Process")



Item		Warpage(mm) After PMC
400ZHF40W	With repair process	0.10
	No treatment	1.05

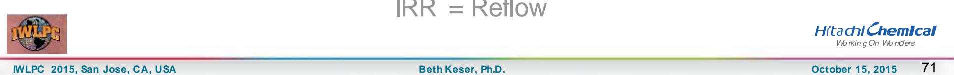
- Relaxation occurs during anneal treatment
- Warpage is reduced >900μm

Warpage Relaxation with Repair Process

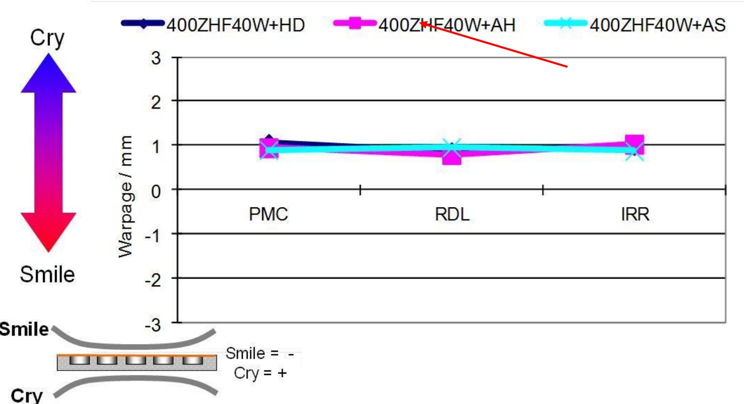


- Warpage flat with anneal treatment throughout FOWLP process

IRR = Reflow



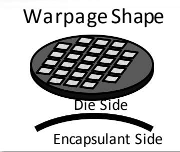
Warpage without Repair Process

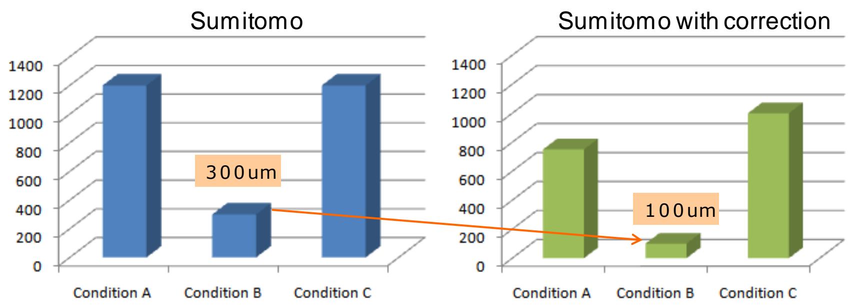


- Warpage minimal without anneal treatment

Warpage with Repair Process

Warpage Correction can minimize final panel warpage

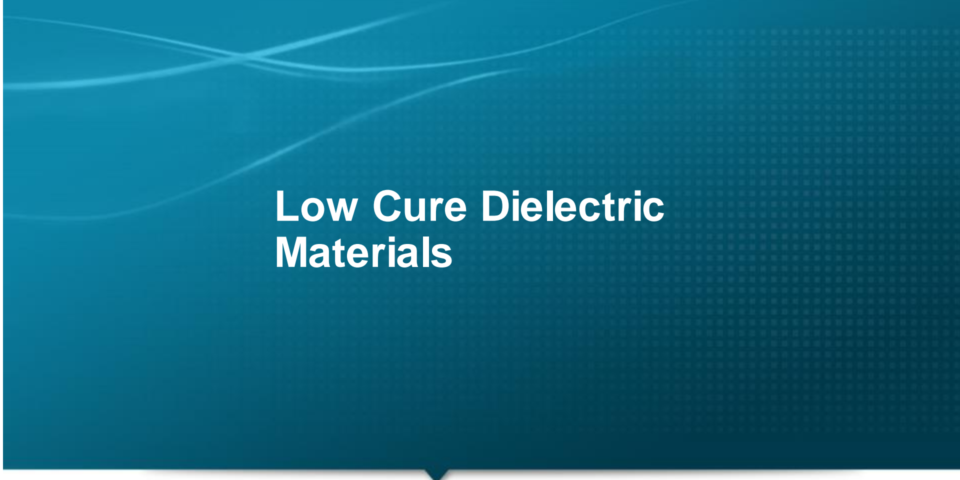




SUMITOMO BAKELITE CO., LTD.

EMC Material Properties

	Hitachi	Nagase	Panasonic	Sumitomo
Material	Solid	Liquid	Liquid	Solid
Filler Loading (wt%)	85	89	88	90
Maximum Filler Size (µm)	54	75	25	55
Viscosity (Pa s)	NA	600	300	NA
Mold Condition	10 min / 125°C	10 min / 125°C	10min / 125°C	7 min / 125°C
Post Cure	1 hour / 150°C	1 hour / 150°C	1 hour / 150°C	1 hour / 150°C
Tg (°C)	160	165	150	170
Flexural Modulus (GPa)	23.5	22	22.5	30
CTE1 (ppm/°C)	7	7	10	7
CTE2 (ppm°/C)	26	30	40	28



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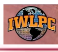
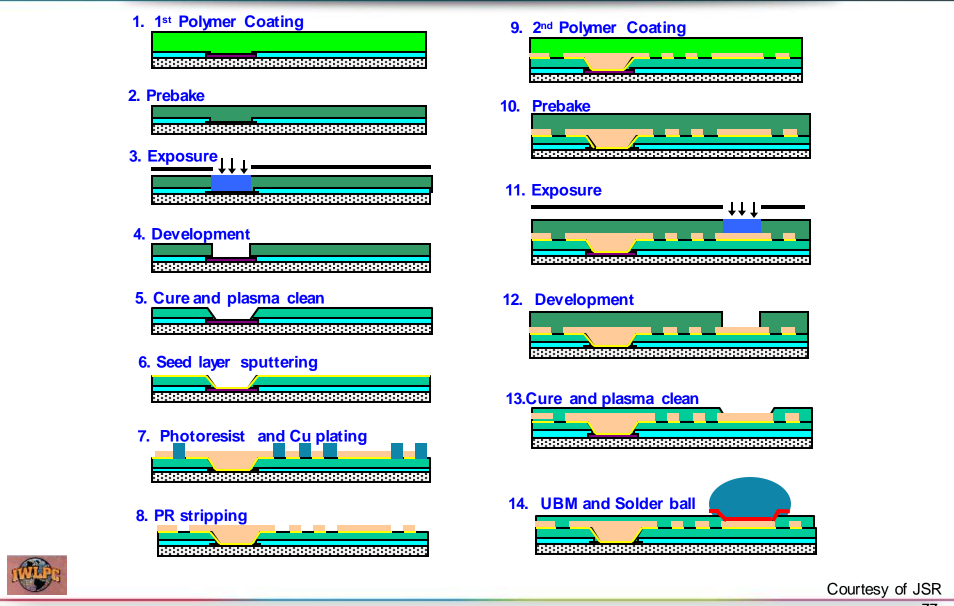
Dielectric Material Challenges for FOWLP

- Cure temperature
  - <230°C due to molded wafer
- Low warpage
  - Low film stress
  - Low Elastic modulus
- Reliability
  - Low modulus
  - High elongation
- Chemical Resistance
- Adhesion
- Planarization
- Via resolution



Dielectric Process Flow (Positive material)



Material Characteristics

Typical Photosensitive PBO

-CONH, NHCO, HO, OH, R — cure, $-H_2O$ → N, O, R

Polybenzoxazole precursor → Poly benzoxazole (PBO)

Typical Photosensitive Polyimide

H, O, N, C, RO, C, OR, X — cure, $-H_2O$ → N, O, X

Low temperature cure can be achieved by tailoring polymer structure (R, X) and additive optimization.

Material Characteristics

PBO

BCB

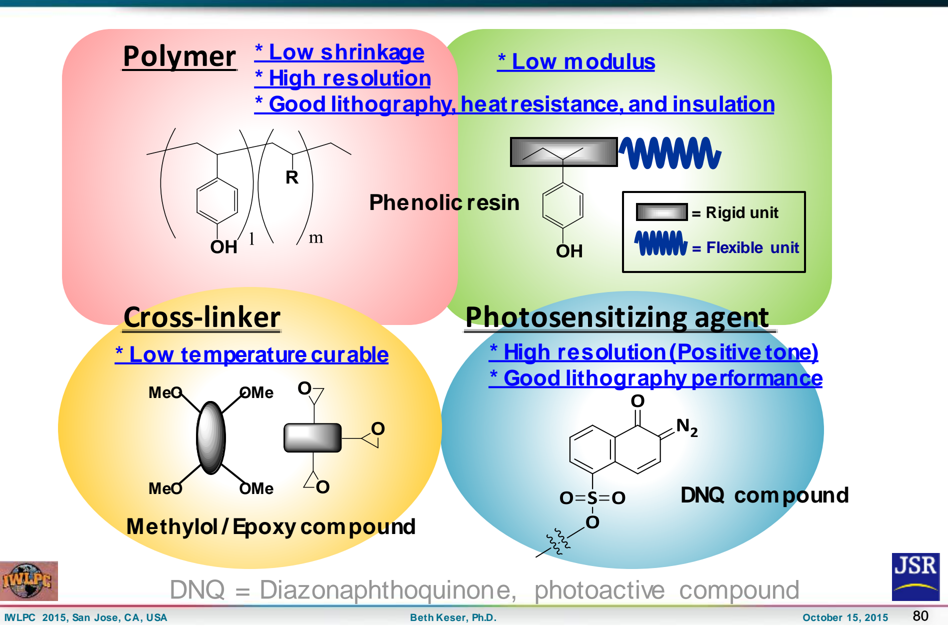
R

PI

Phenolic Resin

Cyclic olifen

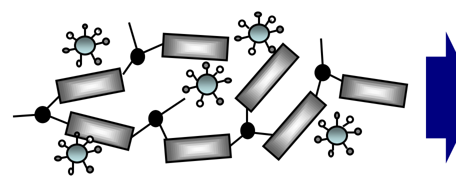
Designing a Low Temp Cure Phenolic Resin

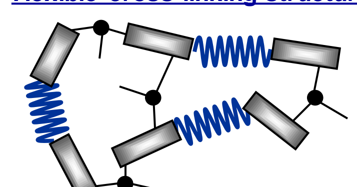


Epoxy Dielectric Material Properties

Design Concept for Low Modulus

Flexible cross-linking structure

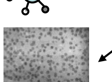




= *Rigid unit* ● = *Cross-linker*

= *Rubber particle*

= *Flexible unit*



Cross-linking rubber particle
(Particle size : ca.70nm)

● : Alkaline solubility unit
O : Compatible unit

- ✓ Flexible unit in cross-linking network
- ✓ Higher loading amount
- ✓ Uniformed dispersion in network

Low modulus
< 2.0GPa

Challenges

Challenges of Low-Cure Photoimageable Dielectric Design	
Process conditions	Dispense Volume
	Coating Uniformity
	Film Thickness Range
	Photospeed
	Resolution
	Particle Defectivity
	Purity
	Cycle time
Material Properties	Thermo-mechanical Properties (Tg, CTE, E, wt% degradation)
	Mechanical Properties (E, elongation, strength)
	Electrical Properties (dielectric constant and dielectric loss)
	Chemical Resistance
	Adhesion
FO-WLP Compatibility	Spin-coating
	Exposure Type (broadband, i-line, laser)
	Warpage
	Thermal budget

- **EHS Friendly**
- **Cost**
- **Previous IP**

Low Cure Dielectric Properties

	HD4100 (REF)	HD8820 (REF)	JSR WPR-5100	Sumitomo CRC-XXXXX	DOW 8005	Zeon ZC100-T
Polymer	polyimide	PBO	phenolic resin	PBO	BCB	Olefin
Tone	negative	positive	positive	positive	positive	positive
Cure T (ºC)	350-390	300-350	200	220	200	180
CTE (ppm/ºC)	35	60	50	39	65	51
Elongation (%)	45	100	15	55	28	8
Tg (ºC)	325	300	219	283	>300	196
Young's Modulus (GPa)	3.5	2.3	1.8	2.7	2.0	2.9
Tensile Strength (MPa)	200	170	110	124	98	100
Residual Stress (MPa)	34	37	16	25	25	23
Dielectric Constant	3.2	2.9	3.5	3.5	3.0	2.9
Water Absorption (%)	1	0.5	1.3	1.4	1.2	0.18

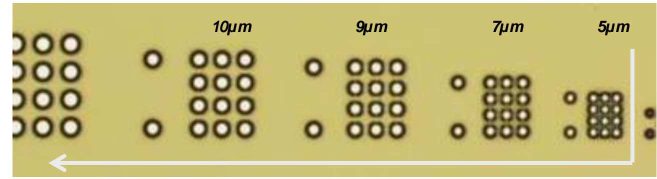
Process Characteristics: PBO

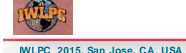
Coating Material			Sumitomo PBO CRC-X2	HDMicrosystems HD8930
Process		Unit		
	Coating	rpm x sec	800 x 10 + 2310 x 25 + 1500 x 5	3000 x 30
	Prebake	ºC x min	125 x 4	120 x 3
	Film Thickness	µm	7.3	7.5
	Exposure	mJ/cm2	420-630 (aligner)	240 (stepper)
	Developer		2.38% TMAH	2.38% TMAH
	Puddle	sec	30	2x30
	Film Thickness	µm	5.8	5.7
	Thickness Loss	µm	1.5	1.8
	Curing	degC x min	200 x 90	200 x 60
Cured Film Thickness (µm)			5.0	4.9

courtesy of Sumitomo, HDM

Resolution: Sumitomo PBO

5μm thick film



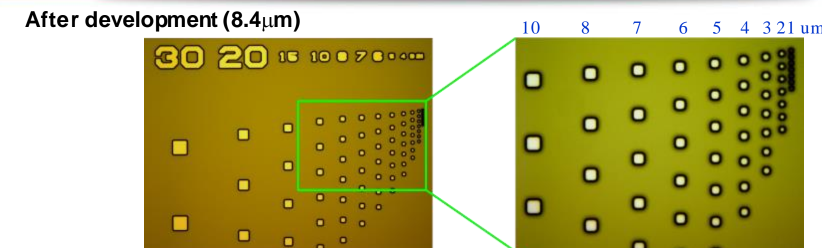


SUMITOMO BAKELITE CO., LTD.

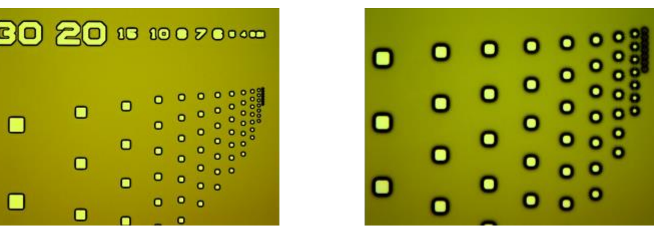
Resolution: HDM PBO

After development (8.4μm)

10 8 7 6 5 4 3 2 1 um



After Cure (7.1μm)

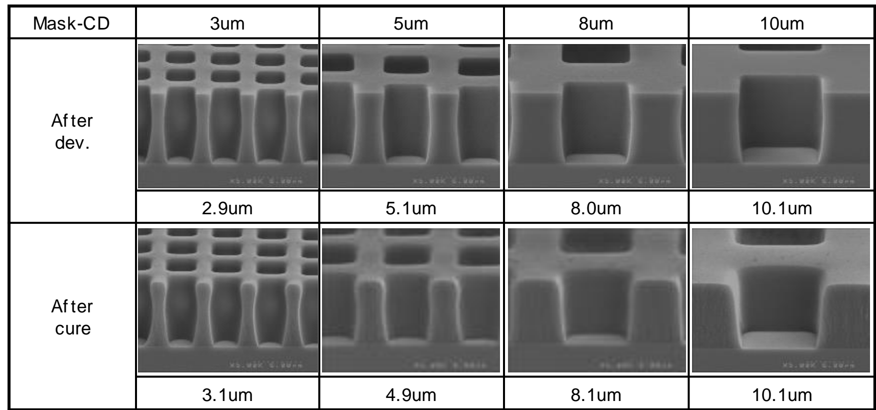


Cure: 200C/1hr

2um opening

HD MicroSystems

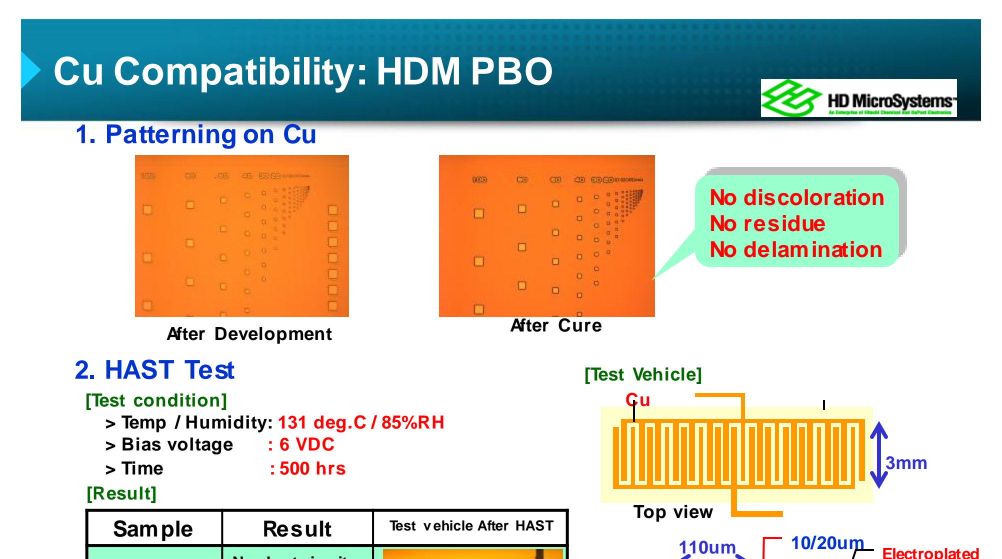
Resolution: JSR Phenolic Resin



Mask-CD	3um	5um	8um	10um
After dev.	2.9um	5.1um	8.0um	10.1um
After cure	3.1um	4.9um	8.1um	10.1um

3um via at 10um cured film thickness.

Cu Compatibility: HDM PBO



1. Patterning on Cu

2. HAST Test

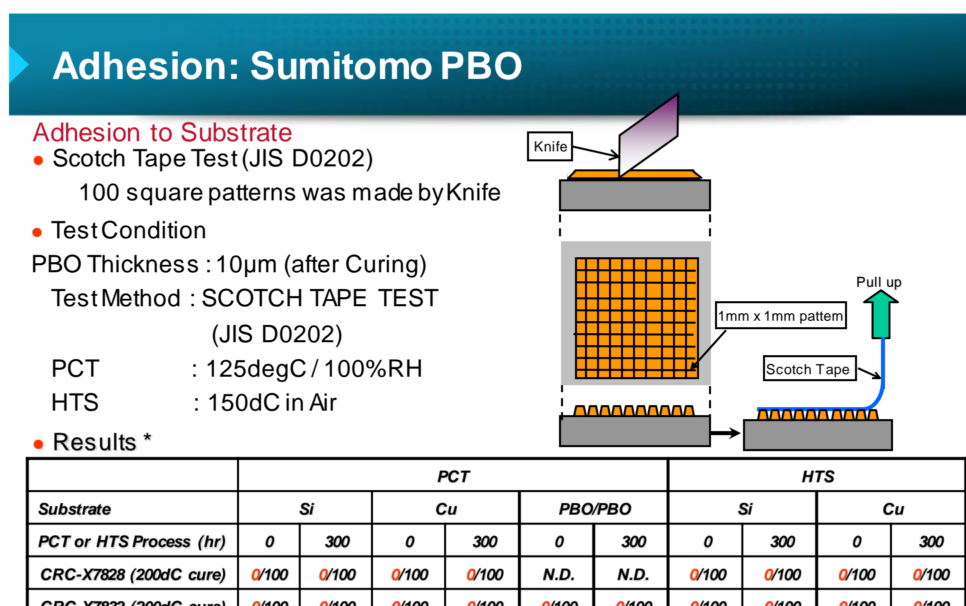
[Test condition]

- > Temp / Humidity: 131 deg.C / 85%RH
- > Bias voltage : 6 VDC
- > Time : 500 hrs

[Result]

Sample	Result	Test vehicle After HAST
PBO (200ºC cure)	No short circuit No dendrite No corrosion No delamination	

Adhesion: Sumitomo PBO



Adhesion to Substrate

- Scotch Tape Test (JIS D0202)

  100 square patterns was made by Knife

- Test Condition

PBO Thickness : 10μm (after Curing)

Test Method : SCOTCH TAPE TEST (JIS D0202)

PCT : 125degC / 100%RH

HTS : 150dC in Air

- Results *

	PCT						HTS			
Substrate	Si		Cu		PBO/PBO		Si		Cu	
PCT or HTS Process (hr)	0	300	0	300	0	300	0	300	0	300
CRC-X7828 (200dC cure)	0/100	0/100	0/100	0/100	N.D.	N.D.	0/100	0/100	0/100	0/100
CRC-X7832 (200dC cure)	0/100	0/100	0/100	0/100	0/100	0/100	0/100	0/100	0/100	0/100

*(Number of peel off / Total number of squares)

PCT = Pressure Cooker Test, HTS = High Temp Storage

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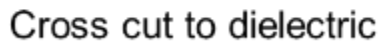
Adhesion: HDM PBO to Hitachi EMC

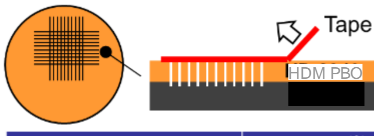
HDMicrosystem's PBO

Cross-section of FOWLP

Cross cut test



Cross cut to dielectric



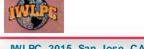
Condition		Result ※
Pressure Cooker Test	100 h	100/100
	300 h	100/100
	500 h	100/100

※100/100: all pieces remained after the testing (No failure)

SEMICON Taiwan 2014
Masaya Toba, Hitachi Chemical CO., Ltd

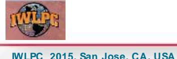
Chemical Resistance: Phenolic resin

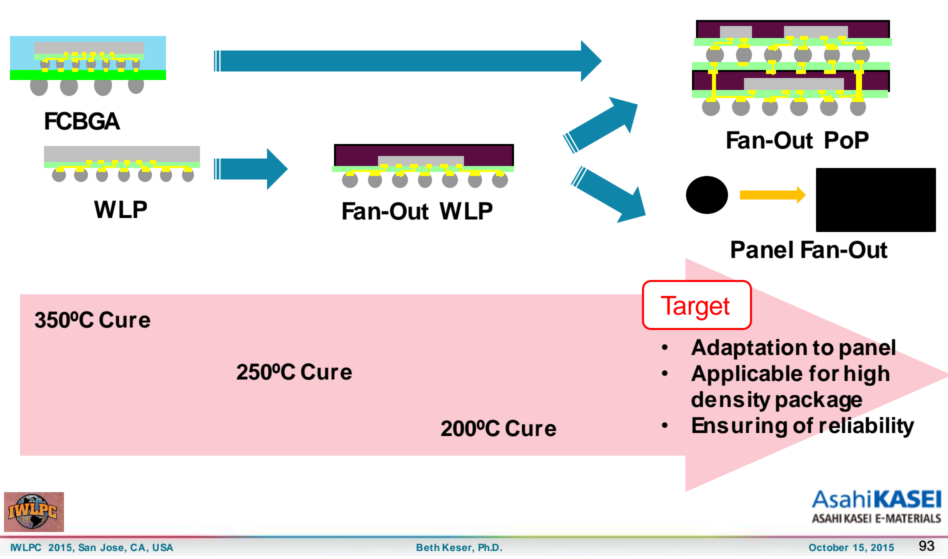
Chemicals	Conditions	New
PGME/PGMEA	r.t./10min	pass
PGMEA	40°C/10min	pass
NMP	r.t./10min	pass
	40°C/10min	pass
DMSO	r.t./10min	pass
PR stripper (TMAH/DMSO)	r.t./10min	pass
	40°C/10min	pass
IPA	r.t./10min	pass
	40°C/10min	pass
Hydrofluoric acid aq. (0.5%)	r.t./5min	pass
Sulfuric acid aq. (10%)	70°C/5min	pass
Sodium hydroxide aq. (7%)	r.t./30min	pass
TMAH (2.38%)	r.t./30min	pass



Reliability

- Dielectric Cracking Concern
  - Lack of elongation of dielectric material causes crack during thermal cycle test.
  - Elongation is small during cooling.
    - When multiple thermal deformations become larger than the film elongation, the dielectric cracks.




Low Cure Dielectric Roadmap
FCBGA
WLP
Fan-Out WLP
Fan-Out PoP
Panel Fan-Out
350ºC Cure
250ºC Cure
200ºC Cure
Target
• Adaptation to panel
• Applicable for high density package
• Ensuring of reliability
AsahiKASEI
ASAHI KASEI E-MATERIALS
IWLPC 2015, San Jose, CA, USA
Beth Keser, Ph.D.
October 15, 2015
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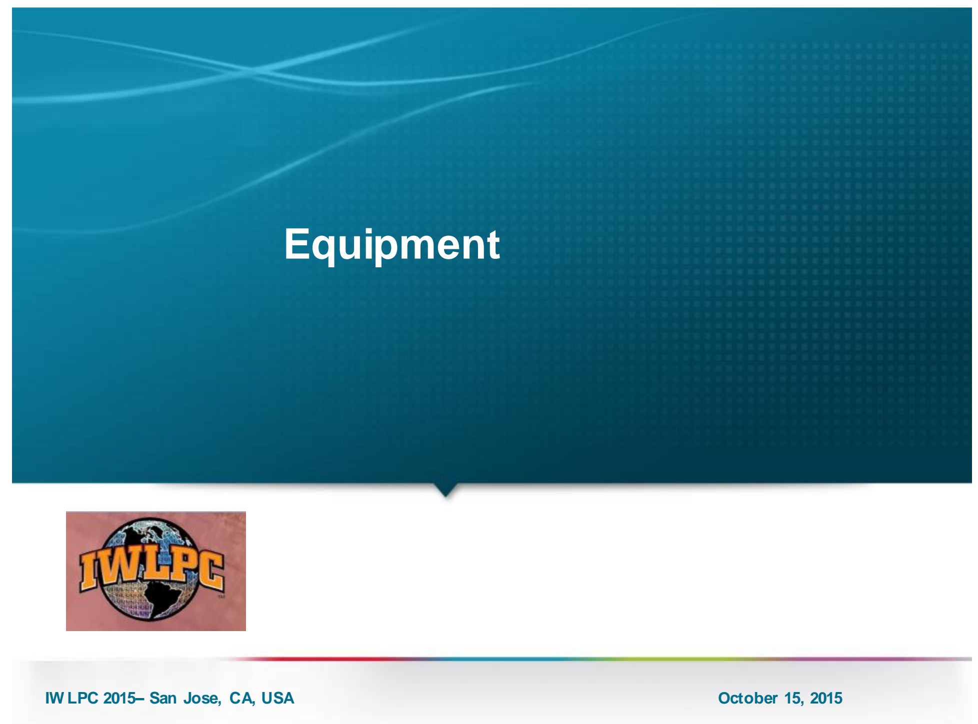
Equipment
IWLPC
IW LPC 2015– San Jose, CA, USA
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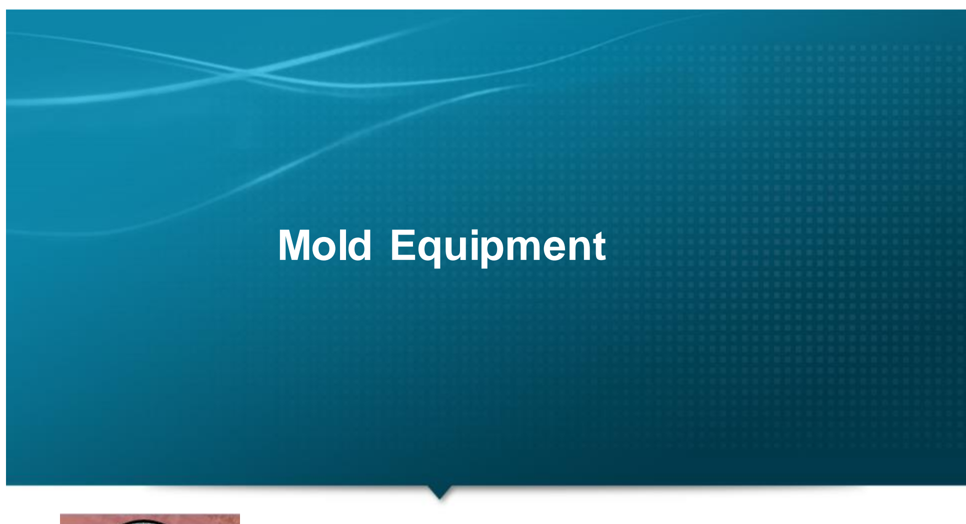

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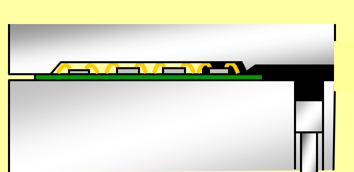
Compression Molding vs. Transfer Mold

- Traditional packaging

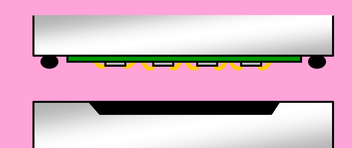
Transfer Mold Technology



Transfer Molding Process

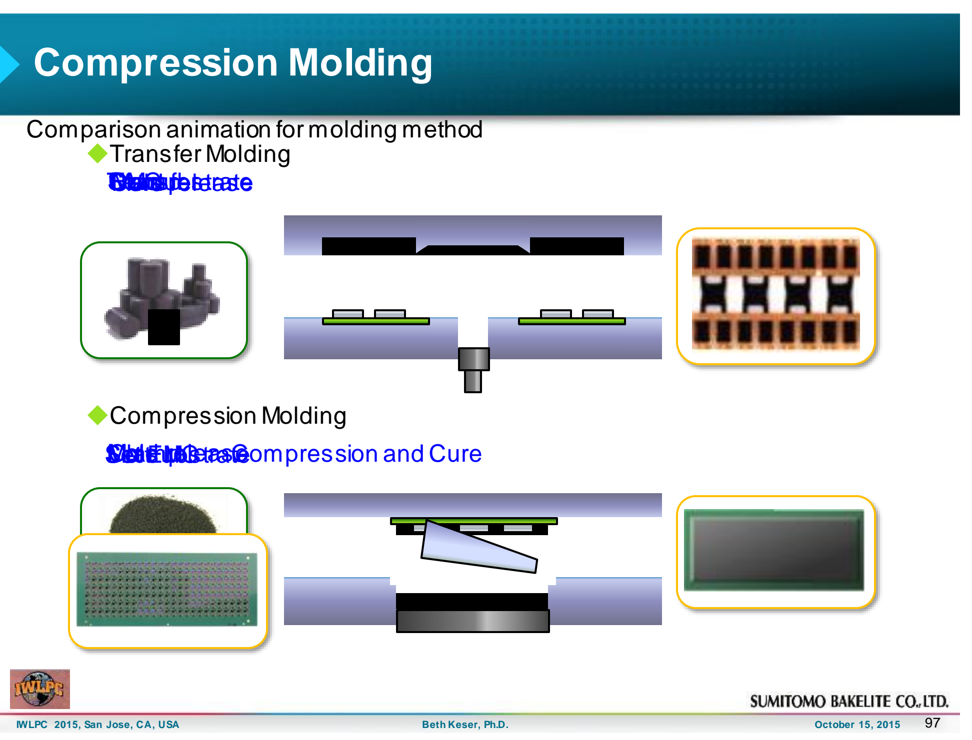
- Pellet in to the pot, then melting resin
- Push in to the cavity by plunger
- Resin flow speed is 3～15 mm/sec

Compression Mold Technology



Compression Molding Process

- Resin is loaded in to cavity that has film laid over on bottom mold.
- Substrate held upside down on top mold.
- Bottom mold move up to gently close.


Compression Molding
Comparison animation for molding method
Transfer Molding
Compression Molding
Compression and Cure
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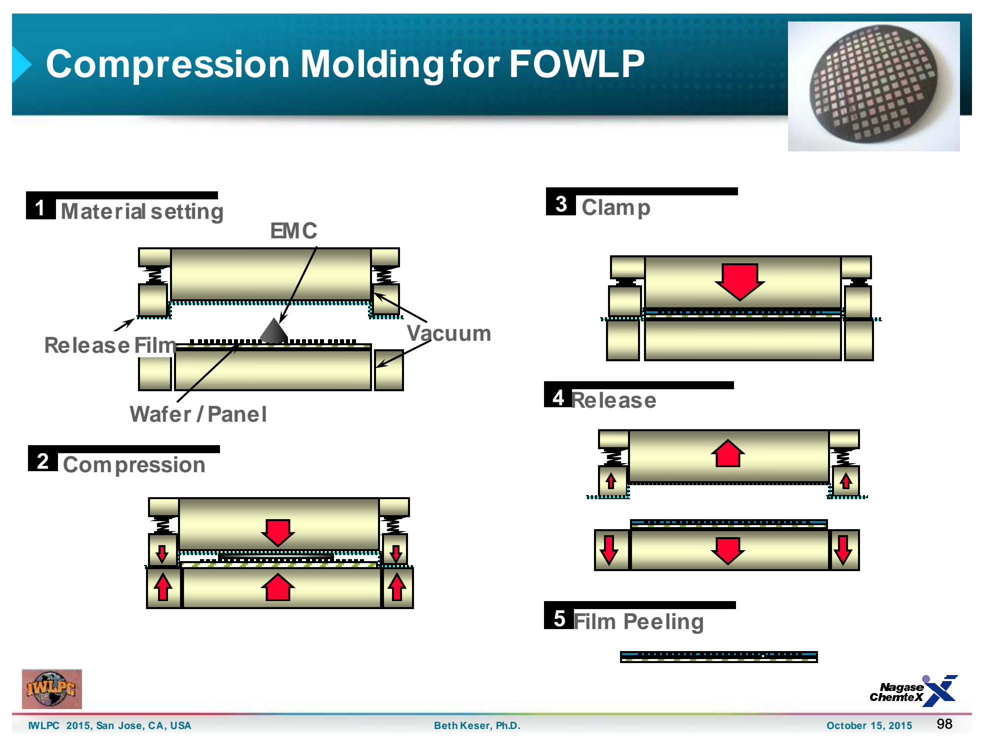
Compression Molding for FOWLP
1 Material setting
EMC
Release Film
Vacuum
Wafer / Panel
2 Compression
3 Clamp
4 Release
5 Film Peeling
Nagase ChemteX
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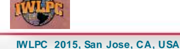
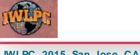
Advantages of Compression Mold

- Minimum packing pressure
- Thinner and smaller packages
- Minimize mold compound cost, waste, storage
  - No runners
- Scales up to large panel size
- Minimum tooling changes minimizes process disruption
- Release film covers top mold chase
  - Obsoletes cleaning and conditioning



Compression Molding vs. Transfer Mold

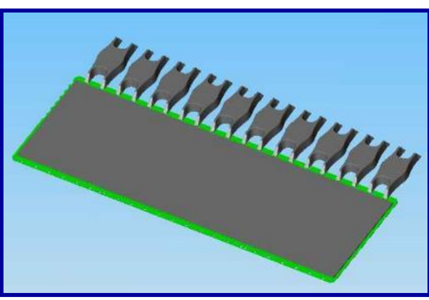
	Compression Mold	Transfer Mold
Compound usage	100%	Around 70%
Reliability, Warpage	Better due to even filler distribution	Filler distribution uneven
Moldability (Thin mold cap and large substrate w/o void)	Very good Scalability	Limited
Flexible Package Thickness	Mold recipe change	Tool change required

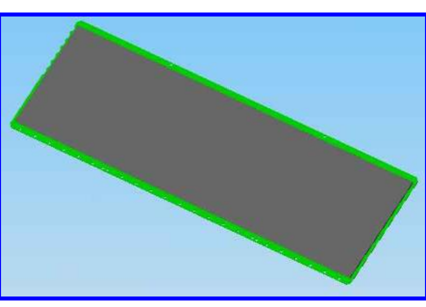


Mold Compound Usage

Transfer Molding

Compression Molding

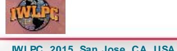




Approx. 70% resin usage

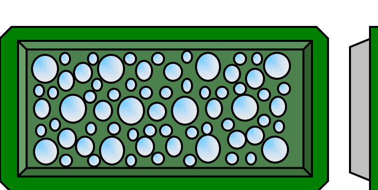
100% resin usage

Improved resin utilization and reduction of waste material and disposal cost

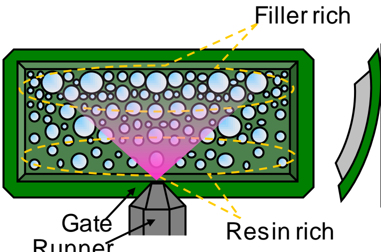


Filler Distribution Comparison

Compression Mold



Transfer Mold

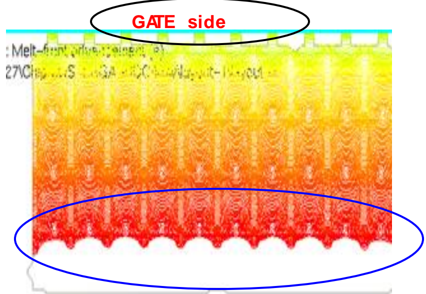


- No mold flow due to EMC transfer
- Filler distribution even

- Filler separation due to mold flow
- Uneven filler distribution → warpage, reliability issues

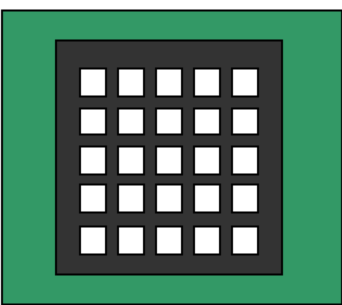
Moldability: Thin mold cap and large substrate without voids

Transfer molding



Compound flow unbalance

Compression molding

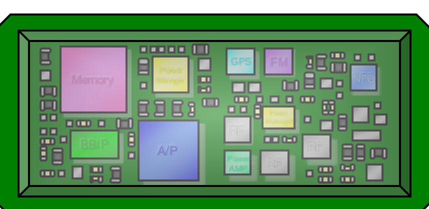


Compound flow-free

- Transfer Molding takes longer time to fill mold
- Compression molding pre loaded mold compound enables larger panel molding

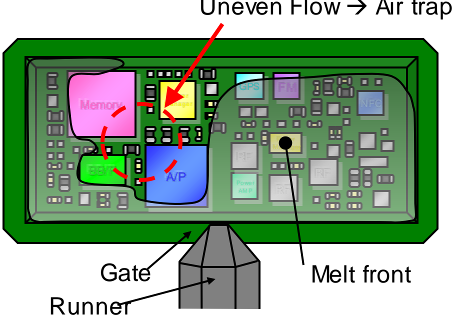
Moldability (Module device w/o void)

Compression Mold



Compression molding with pre loaded mold compound has negligible flow that enables void free molding.

Transfer Mold



Pressurize flow and components of different sizes cause uneven flow resulting in voids/airtrap

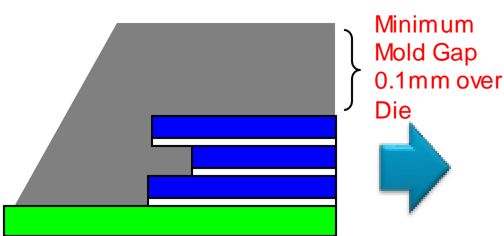
Package Thickness Reduction

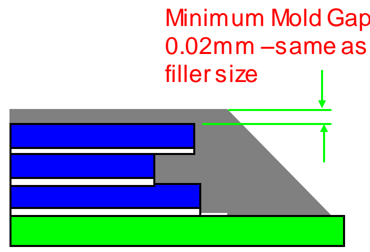
Transfer molding

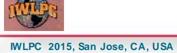
Mold gap necessary for compound flow

Compression molding

Mold gap not necessary



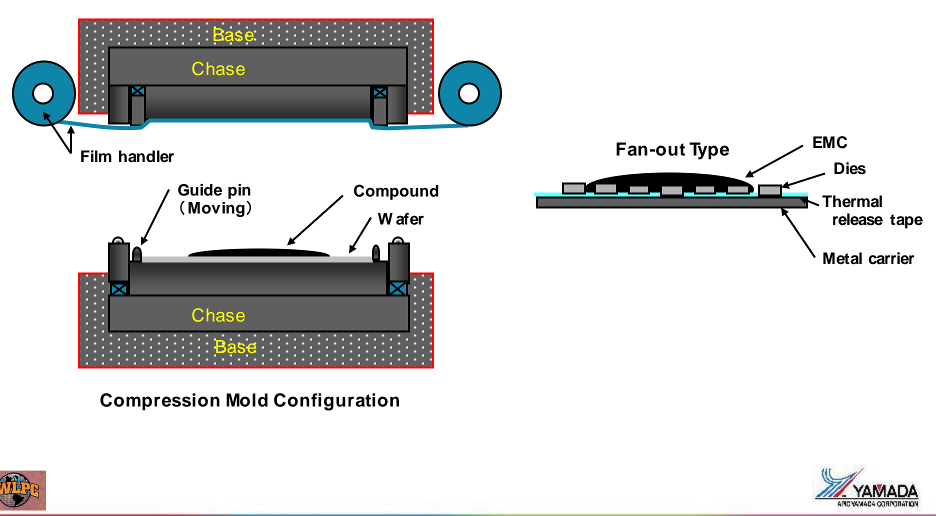




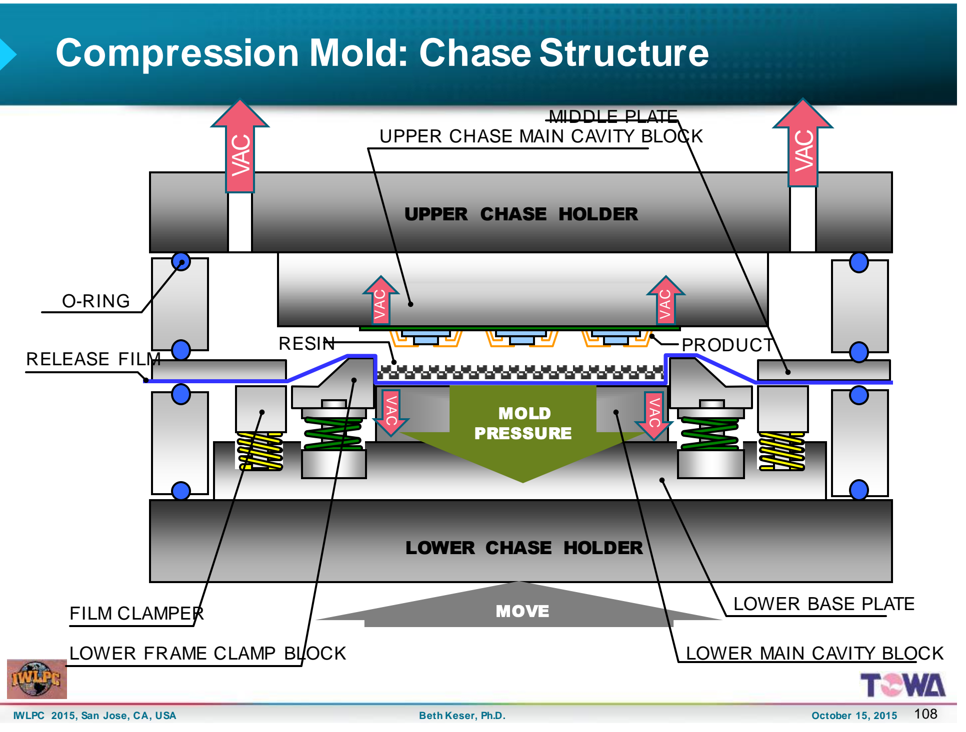
Mold Equipment Challenges

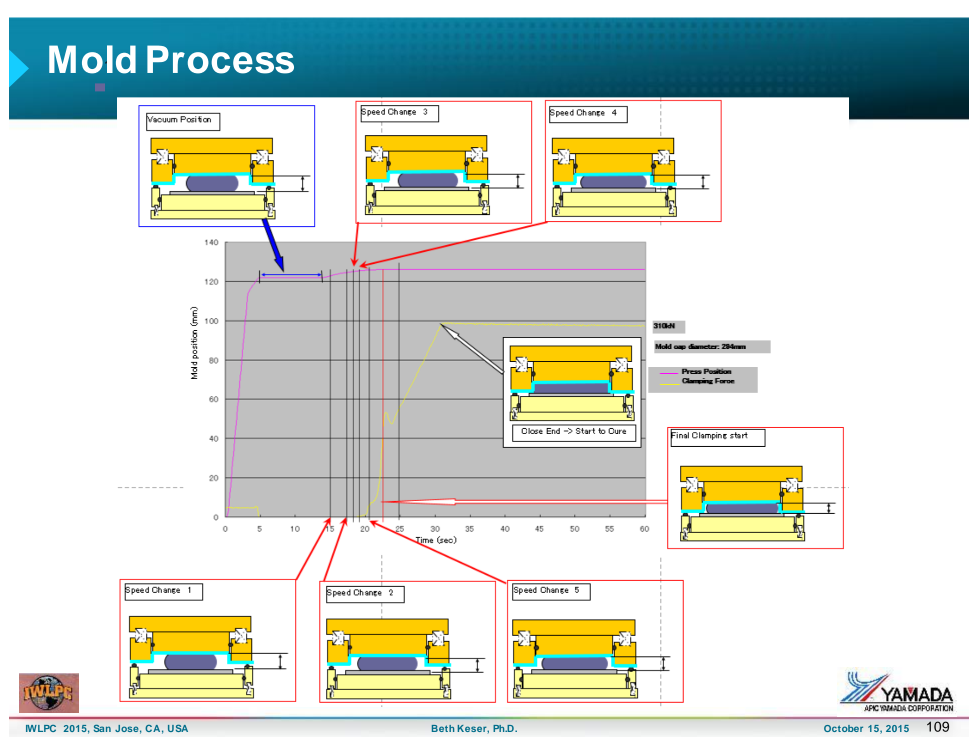
- Capital cost
- Throughput
- Die Drift
- Mold thickness uniformity
- Gap filling
- Handling and dispensing EMC
  - Liquid/pellet/granular/powder

Key Tool Characteristics and Capability



Compression Mold: Chase Structure





Mold Process
Vacuum Position
Speed Change 3
Speed Change 4
Mold position (mm)
140
120
100
80
60
40
20
0
0
5
10
15
20
25
30
35
40
45
50
55
60
Time (sec)
310kN
Mold cap diameter: 294mm
Press Position
Clamping Force
Close End -> Start to Cure
Final Clamping start
Speed Change 1
Speed Change 2
Speed Change 5
YAMADA
APIC YAMADA CORPORATION
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October 15, 2015
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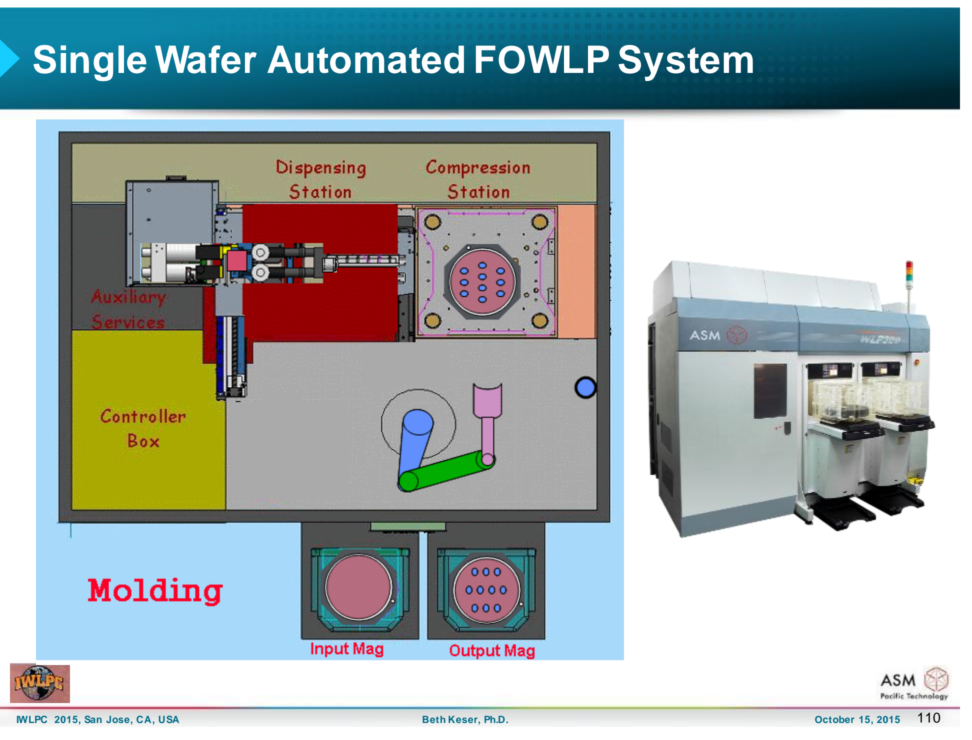

Single Wafer Automated FOWLP System
Dispensing Station
Compression Station
Auxiliary Services
Controller Box
Molding
Input Mag
Output Mag
ASM
ASM Pacific Technology
IWLPC 2015, San Jose, CA, USA
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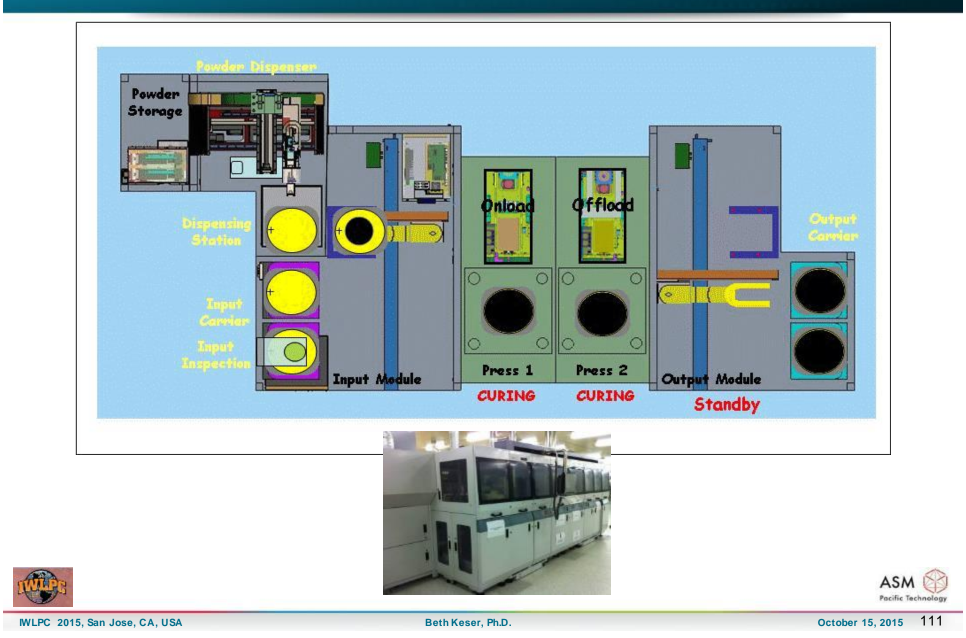
Multi-Press Automated FOWLP System
Powder Dispenser
Powder Storage
Dispensing Station
Input Carrier
Input Inspection
Input Module
Onload
Offload
Press 1
CURING
Press 2
CURING
Output Module
Standby
Output Carrier
ASM Pacific Technology
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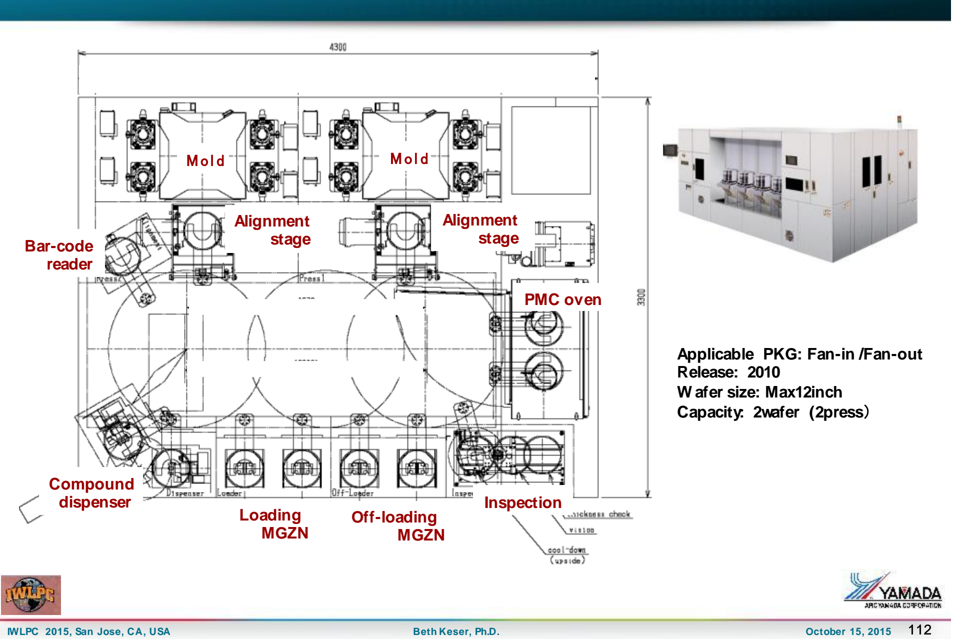
Multi-Press Automated FOWLP System with PMC
4300
3300
Mold
Mold
Alignment stage
Alignment stage
Bar-code reader
PMC oven
Compound dispenser
Loading MGZN
Off-loading MGZN
Inspection
Applicable PKG: Fan-in /Fan-out
Release: 2010
W afer size: Max12inch
Capacity: 2wafer (2press)
YAMADA
IWLPC 2015, San Jose, CA, USA
Beth Keser, Ph.D.
October 15, 2015
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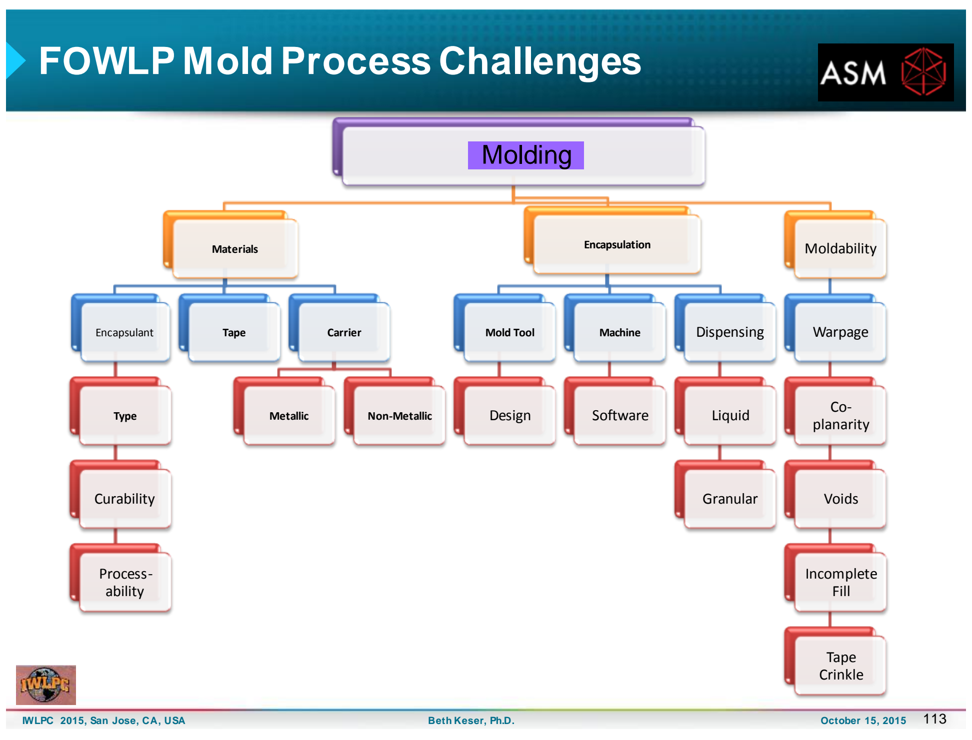
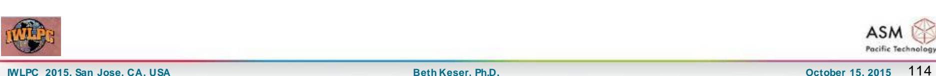


Molding Process Challenges

Challenges	Defects	Root causes	Counter Measures
Void / Incomplete fill		Air trapped in package	• High vacuum to evacuate air from molding chamber • Optimize molding parameter
Flow mark		Uneven distribution of filler and resin	• Reduce compound flowing as much as possible • Improve consistency in dispense
Warpage		Molding compound and substrate CTE mismatch	• Match CTE between EMC & Substrate • Mold at as low as possible temperature
Bleeding		Insufficient clamping area or wrong parameters used	• Improve mold design • Optimize molding parameter

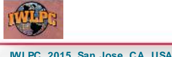


System Design Challenges

- Press capacity
- Mold coplanarity
- Platen deformation
- Packaging versatility
- Vacuum design

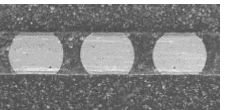
Press Capacity

- In compression molding, mold area is much bigger than clamping area, therefore most capacity goes for resin packing
  - E.g. in 12” wafer molding, clamping and packing area is $25cm^2$ and $680cm^2$ respectively
- Required packing pressure is another important factor to determine press capacity

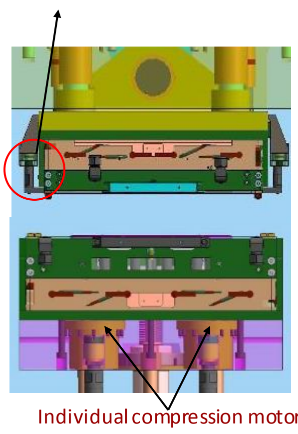


Typical Required Packing Pressure

- Clear epoxy/silicone molding
  - 10-20kg/cm²
- Over mold of simple devices
  - 30-40kg/cm²
- FOWLP/thin packages/ball exposure/MUF (molded underfill)
  - 40~50kg/cm²
- Ultra thin package and fine pitch MUF
  - > 60 kg/cm²



Platen: Sensing for Co-planarity



- Mold Press
  - Driven by precise servo motors with 60 ton capacity
  - Auto compensation enabling mold coplanarity within 20μm
  - Maximum number of press in multiple mold station is 4

ASM Pacific Technology

Vacuum Design

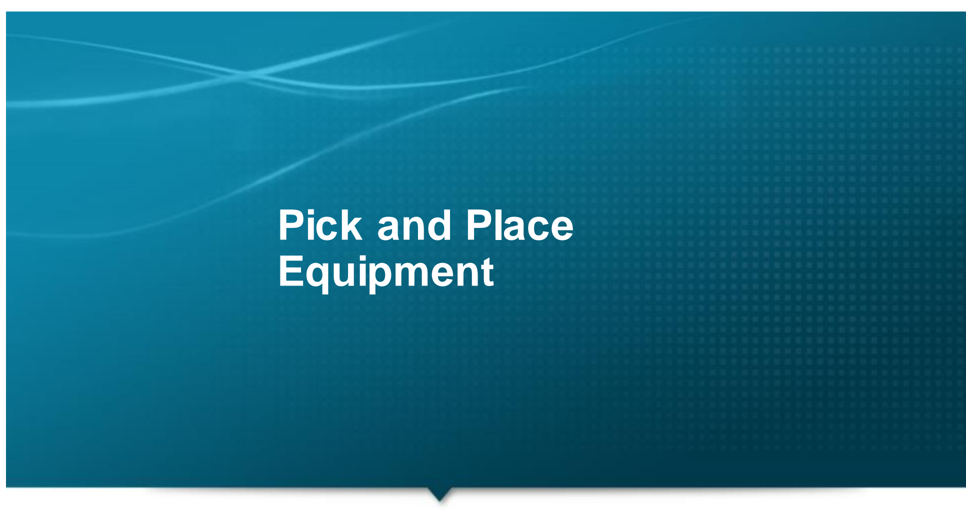
- Vacuum performance is critical for wafer level molding
  - Minimum mold flow does not facilitate air escape
  - Large packaging area, so potential for air entrapment
  - Die to die spacing needs to be filled
- Sub-torr vacuum can be achieved by high efficient pump, qualified sealing material and methodologies
  - Vacuuming rate control is also important to ensure required vacuum level is achieved

Throughput

Operation	Yamada	ASM
Machine time (mold open/close)	75 sec	30 sec
Cure Time	600 sec	600 sec
Total Cycle Time	675 sec	630 sec
Shots/mold	5.3	5.7
Molds/system	2	2 (4max)
Wafers per Hour	10.6	11.4 (22.8)

Compression Mold Tool Comparison

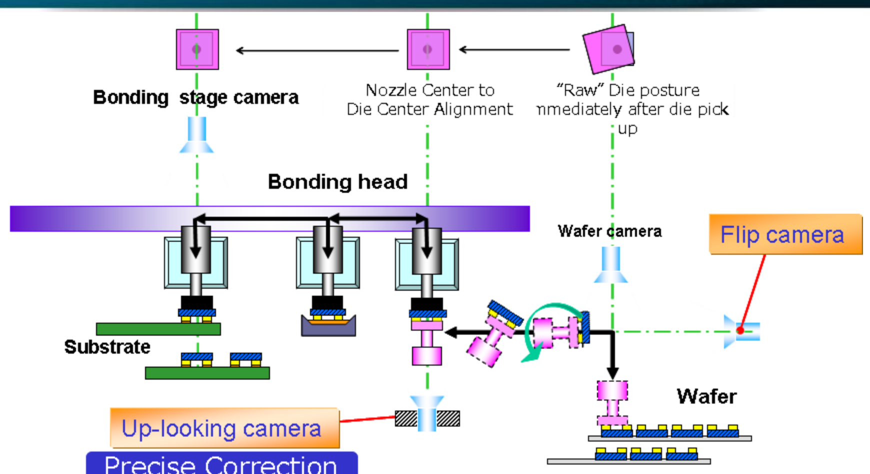
Vendor	Compound Types	Price	Market - General	Market - FO
ASM Pacific Technology	Liquid and Solid	++	++	++
TOWA	Liquid and Solid	++	+++	+
YAMADA APIC YAMADA CORPORATION	Liquid and Solid	+	+	+++



Placement Equipment Challenges

- Placement Accuracy
- Fiducials: local vs. global
- Throughput
- Handling
- Capital Cost
- Feeders

Flip Chip Bonder/Pick and Place



Flip Camera insures good alignment between Bonding Head Nozzle Center and Die Center during transfer

Panasonic

Assembleon Pick and Place Video

Placement Challenges

- **Local Accuracy**
  - There are fiducials on the substrate next to the bond location
  - With every bond the machine can align on the local fiducials before die placement
  - Between alignment and bond there is usually less than a second of time
- **Global Accuracy needed for FO-WLP**
  - There are no fiducials on the substrate next to the bond location
  - The machine can only align once on global fiducials
  - After the global alignment the machine has to build-up a consistent matrix of dies without a possibility of local alignment
  - Between alignment and bond there can be hours of time
- **Multi Bond Head Machines (needed for FO-WLP!)**
  - To provide sufficient UPH (units per hour) the pick & place machine needs to have multiple bond heads
  - The combination of global accuracy and multiple bond heads is an additional challenge, as the offset drift between different bond heads needs to be under control

Besi

Placement Tools

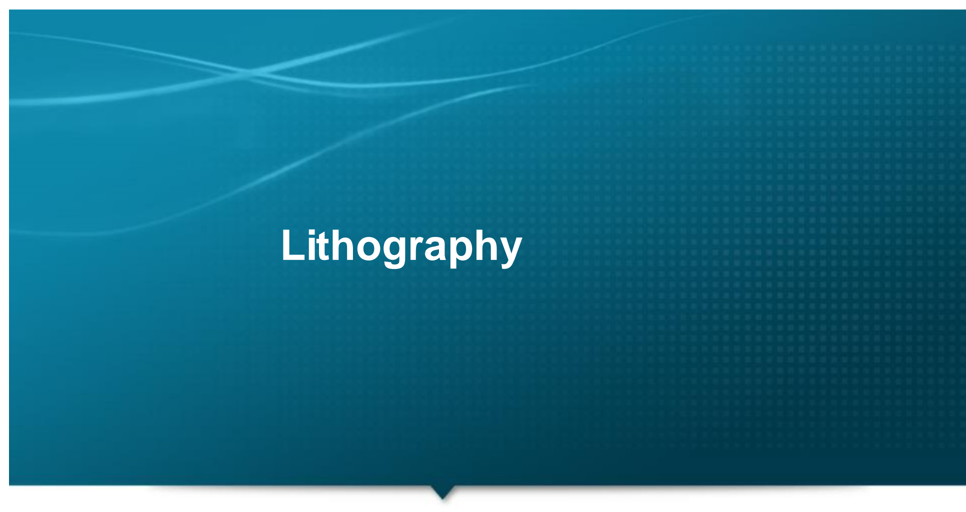
Vendor	Model	Placement Accuracy	UPH	Cost	Work Area
Datacon (BESI)	Datacon 8800 Chameo	±10μm @ 3σ	5000-7000	++	340mm x 340mm
Universal	Fuzion	±10μm @ 3σ	7000-8000	++	813mm x 610mm

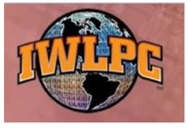
Other Pick and Place Tool Attributes

- Working area (mm)
- # placement heads and spindles/head
- Bond force (N or g)
- Bond force resolution (N or g)
- Part Feeder types
  - Wafer, tape and reel, tray, waffle pack
- Face up and face down placement
- Camera locations, models, and inspection capability
- Max chip size (mm)
- Bond head/stage heater

Spindles/head

Merschon, UIC, IWLPC, 2014





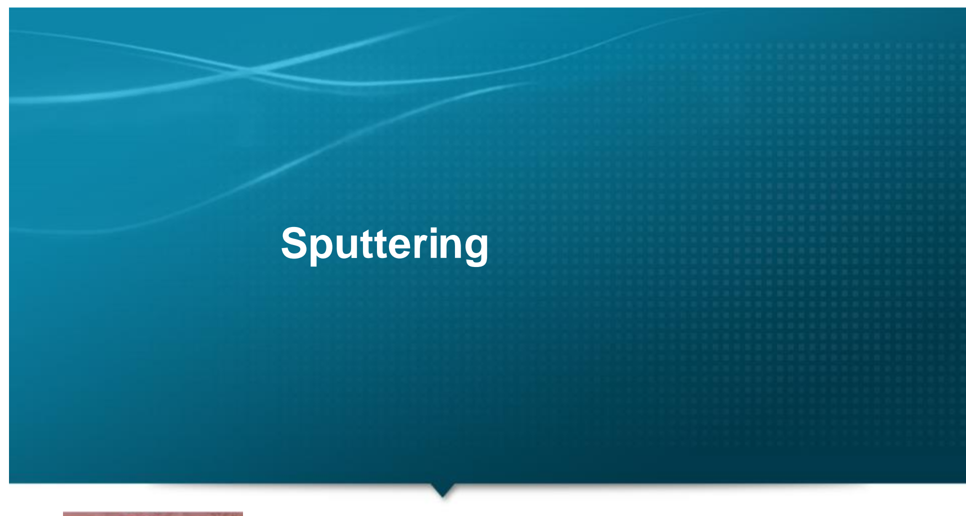
Lithography Challenges

- Warped Molded Wafers
  - Handling
  - Focus
- Depth of focus
- Throughput
- Aligner vs. Stepper
  - Aligner cannot be used due to die drift and panel warpage
    - Poor alignment to die across entire panel results in low yield
  - Stepper images reticle steps across molded panel
    - Can optimize exposure within molded panel, but not within reticle
    - “Quasi-local” alignment

Rudolph JetStep

Feature	Benefit
Large Field of View (52mm x 66mm)	Throughput Maximized (vs. 52mm x 34mm)
On the fly auto-focus	Exact focus on every exposure beneficial for warped wafers
2µm resolution, 0.5µm overlay	Fine via, L/S resolution
Single sided telecentric lens	Real time automatic magnification compensation compensates for die drift
Handling warped molded wafers	Transport and chuck can handle -4mm to +6mm warpage

Stepper Video



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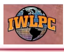
Sputtering Challenges for FOWLP Cu Seed

- Mold compound contains moisture – must be removed
- Mold wafer max temperature is <150°C
- High yield, high throughput FOWLP processing requires:
  - Technology to bake the wafer efficiently
- Multi-Wafer Degas by SPTS
  - Removes degas as bottleneck
- Advantages
  - High Throughput
  - Low Contact Resistance
  - Single wafer processing, single wafer yields



SPTS

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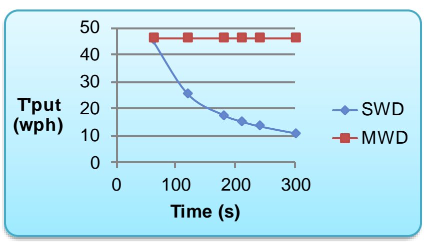
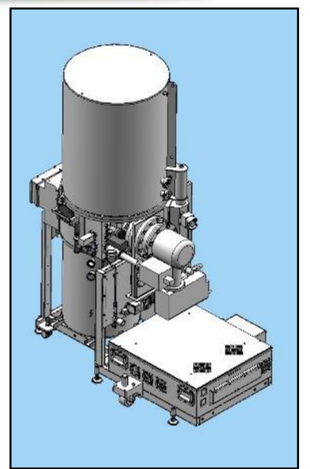
Multi-wafer degas

- Multi-Wafer Degas by SPTS
  - Batch concept, removes degas bottleneck
  - Can degas longer to remove moisture without impacting throughput

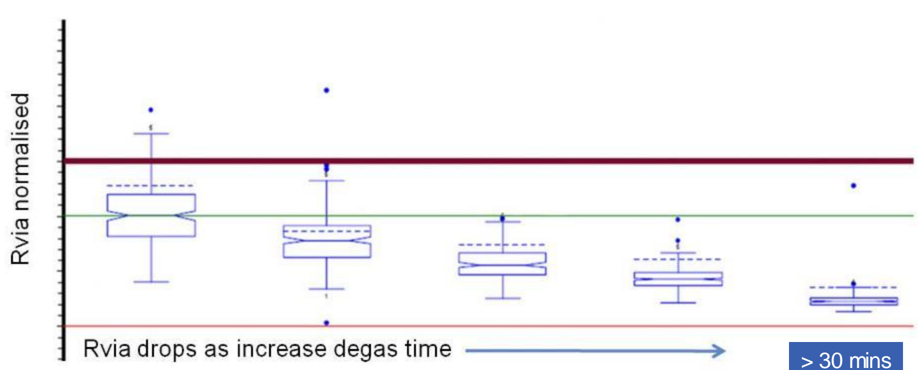




SWD = Single wafer degas
MWD = Multi wafer degas

Contact Resistance vs. Degas Time

Tests performed on FO-WLP Epoxy Mold Compound Test Vehicle
TMAX = 120C



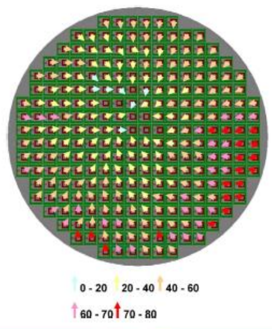
Benefit of batch degas: Longer degas, no loss in throughput

Die Drift Challenges

- For economical and cost effective package, lithography has to be repetitive in HVM.
- Accurate registration of multiple litho layers required.
- Good yield is key enabler for FOWLP.
- Die drift after molding is a well known problem for FOWLP.
- Die drift can lead to significant misalignment in litho processing step.
- Die drift can lead to limit the device pad pitch.
- Die drift can also lead to current crowding and electromigration.

Die Drift

- Mold compound cure shrinkage contributes to die shift.
- Other factors that are attributed to die shift are carrier, tape, adhesive strength, and mold temperature
- Die picked onto tape on a carrier are known to move toward the center of the molded panel.
  - The die shift increases as the distance from center increases

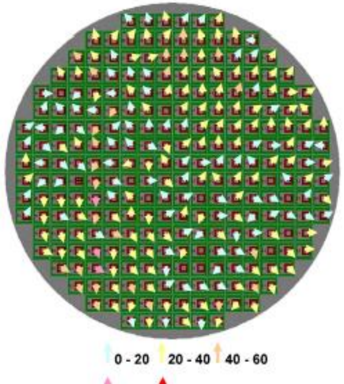


Die shift of 8" molded wafer
7x7 die in 10x10pkg
Max shift of 79um
Mold CTE of 8ppm/ºC
Mold cure shrinkage 0.125%

Sharma, *IEEE Trans. on CPMT*, 2011

Die Drift Optimization

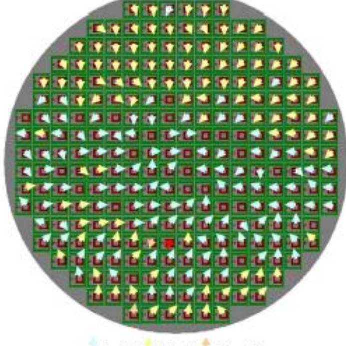
- Compensate for die drift
  - Deliberately misplace die at pick and place to account for drift



100% compensation:
3 die >60um

Die shift of 8" molded wafer after compensation at pick and place

Sharma, *IEEE Trans on CPMT*, 2011



50% compensation:
Only 3 die >40um

Die Drift Optimization

- For same package size, the larger fan out ratio (smaller die size) has larger die drift.
- Lower molding temperature decreases die shift.
  - Reduced ΔT leads to less mismatch between die/tape/carrier
- Lower CTE and cure shrinkage mold compounds can lead to less die drift.
- Other process parameters to reduce die shift: high tape adhesive strength and pre-anneal step after pnp

Sharma, *IEEE Trans. on CPMT*, 2011

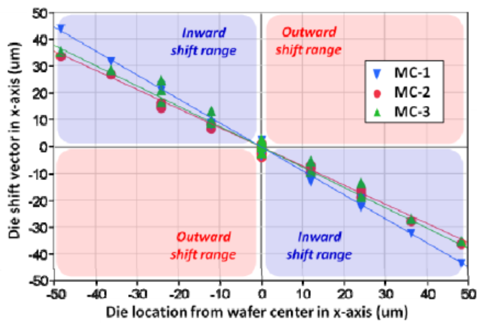
Parameter	Influence on Die Shift	Solution
Molding tape thermal expansion		Use support carrier wafer Use lower molding Temperature
Molding tape adhesive strength		High adhesive strength Use lower molding temperature Pre-anneal molding tape
Mold compound cure shrinkage		Use low cure shrinkage compound
Mold compound thermal shrinkage		Use low CTE mold compound Use lower molding temperature
Die shift pattern		Measure, analyze & compensate

very bad bad very good

Die Drift Impact: EMC Properties

- MC2/3 have higher filler content to increase E and decrease CTE
- MC3 has more catalyst than MC2 to enhance gelation
- Results show that MC1 has higher die drift than MC2/3 likely due to higher CTE2.
- MC2/3 drift is similar.

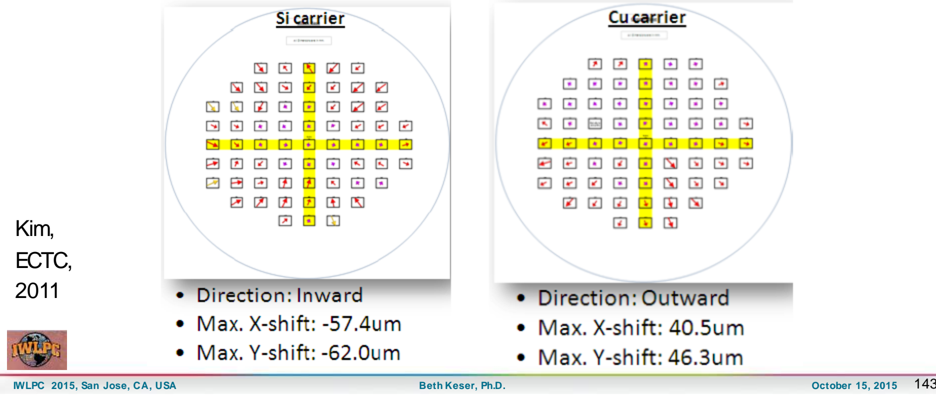
	MC1 (reference)	MC2	MC3
Type	Granule	←	←
Filler (wt%)	89.5	90	←
CTE1/CTE2 (ppm/°C)	7/34	7/31	←
T_g (°C)	143	149	←
Modulus E1/E2 (GPa)	22.6/0.7	24/0.8	←



Kim, ECTC, 2011

Die Drift Impact: Carrier Material

- Si carrier has low CTE of 3ppm/ºC and dimension does not change significantly during mold process. Die drift dominated by cure shrinkage and die move inward.
- Cu carrier has CTE of 17ppm/ºC and expands during mold process causing outward die shift.



Kim, ECTC, 2011

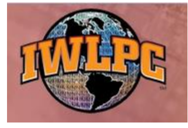
Die Drift Impact: Die/Tape Adhesion

- Typical thermal release tape compared to Brewer Science HT10.10 Wafer bond material (spin on film) which uses thermo-mechanical slide off debond (180-200ºC)
- Pick and place was not compensated

	adhesive film		
	Thermo release		Thermoplastic HT.10.10
pick and place conditions	Applied force (0.15N)	Applied force (0.3N)	Applied force (0.35N) T = 160°C, Time = 5sec
die shear strength (MPa)	80 ± 20	200 ± 20	450 ± 15
die shift (μm)	600 ± 150	30 ± 15	30 ± 15

- By optimizing pick and place parameters to improve adhesion strength between die and adhesive, die drift can be reduced.

Mazuir, EPTC, 2011



General FOWLP Design Rules

Rule	Dimension
Package size	$1x1mm^2 – 25x25mm^2$
Die size	$0.5x0.5mm^2 – 11x11mm^2$
# Cu RDL Layers	2
Cu RDL Line/Space (min.)	10µm/10µm
Die Drift (min.)	15-30µm
Die pad pitch (min.)	40-60µm
Die to package edge (min.)	75µm
Die to die spacing (min.)	150µm
# Die	>3
# Components	>10
Min. Pkg Height (min.)	0.4mm
BGA Pitch (min.)	0.35mm

Nanium Design Rules

Rule	Current	Future
Package size	1x1mm^2 – 25x25mm^2	
Die size	0.2x0.2mm^2 – 10x10mm^2	Larger die will reduce BLR
# Cu RDL Layers	3	
Cu RDL Line/Space (min.)	10µm/10µm	
Dielectric Opening (min.)	15µm	10µm
Die pad pitch (min.)	40µm	
Die to package edge (min.)	50µm	
Die to die spacing (min.)	120µm	80µm
# Die	>3	
# Components	>10	
Min. Pkg Height (min.)	0.35mm	
BGA Pitch (min.)	0.35mm	0.30mm

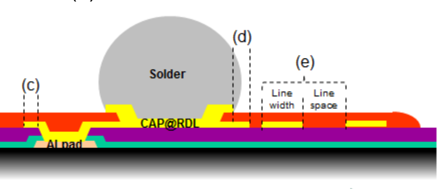
ASE Design Rules

Rule	Current	Comment
Package size	2x2mm^2 – 14x14mm^2	
Die Thickness	0.2mm	
# Cu RDL Layers	3	
Cu RDL Line/Space (min.)	2µm/2.5µm	
Dielectric Opening (min.)	15µm	
PI overlap of die pad opening	15µm	Requires 45µm die pad opening/50µm die pad
Die to die spacing (min.)	100µm	
# Die	>3	
# Components	>10	
Min. Pkg Height (min.)	0.4mm	
BGA Pitch (min.)	0.4mm	

ASE GROUP

Design Rules: ASE

- **Structure Dimensions**
  - Ball pitch/size : 0.4/0.25mm
  - Die thickness : 0.2mm
  - Package thickness : 0.4mm
  - Package size : 2x2 → 14x14mm (3 dies)
  - D2D distance : 0.1mm
- **Connection Geometries**
  - PI thickness : 12um
  - PI opening : 15um (a)
  - Overlap of pad to PI opening : 15um (b)
  - Overlap of metallization to PI opening : 10um (c)
  - Overlap of RDL edge to underbump metallurgy (UBM) edge : 10um (d)
  - Min. line width / space : 2/2.5um (e)
  - Stacked RDL layers : 3



ASE GROUP

J-Devices Panel Level Package (PLP) Design Rules

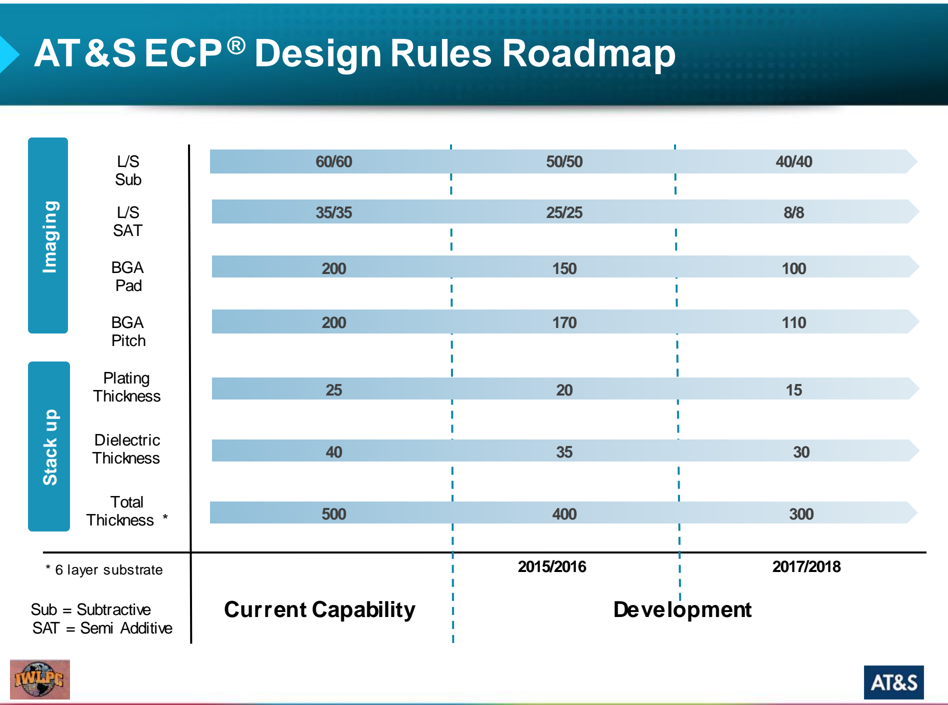
Wafer RDL *Package RDL*

Die
Die pad
PV
PI
Copper Land
L
A
S
B
V0
A
Wafer RDL
Die
E
G
F
D
C

Item		Min. Design rule
Copper land diameter	A	70µm
Die pad pitch	B	55µm
Line width	L	10µm
Space width	S	10µm
Via hole in PI	V0	30µm

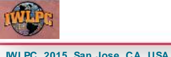
Item		Min. Design rule
Line width	C	20µm
Line space	D	20µm
Via pitch	E	80µm
Via land diameter	F	60µm
Via hole (Top)	G	23µm

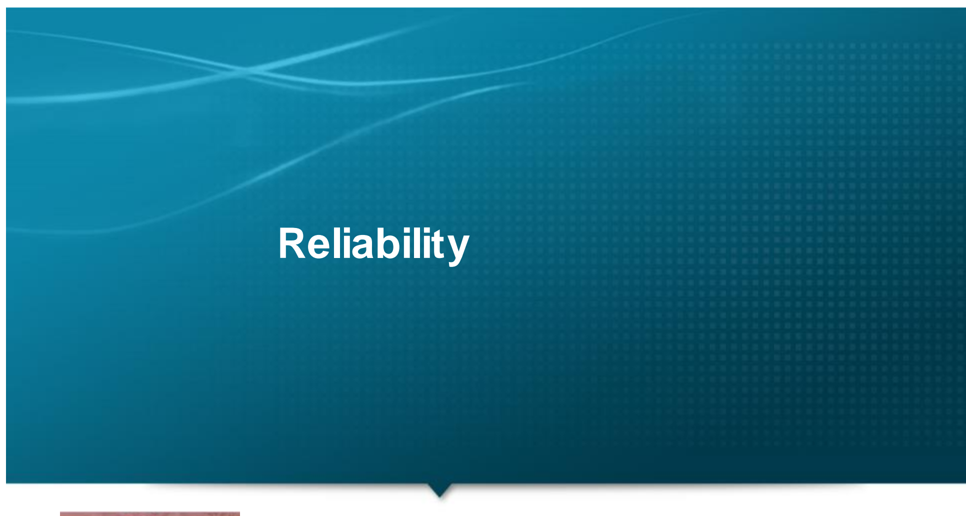
J DEVICES

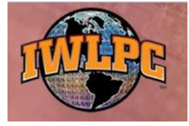


Design Rule Summary

- Wide range of package and die sizes supported
- FOWLP has finer L/S rules than embedded technologies
- Die drift spec is critical to minimize die pad pitch
- Current low cure dielectrics can resolve 15μm via, but highly dependent on polymer thickness
- More specific rules needed for fan-out ratios including any BGA on die/mold compound transition keepout rules







Reliability: eWLB

Stress Test	Standard/ Spec	Pass Criteria
Moisture Sensitivity Level (MSL)	EIA/J-STD-020C (Level 1)	MSL1
High Temperature Storage (HTS)	JESD22-A103 (Ta:150°C)	1000hrs.
Temperature Cycling (TC)	JESD22-A104 (Cond B:-55°C to 125°C) Preconditioned (Level 1; Tr:260°C)	1000x
		1500x
Unbiased HAST(uHAST)	JESD22-A118 Cond A: (130°C / 85% RH) Preconditioned (Level 1; Tr:260°C)	96hrs.
		188hrs.
Temperature Humidity Bias (THB)	JESD22-A101 (85°C / 85%r.h.,VCC)	1000hrs.
Temperature Cycling on Board (TCoB JEDEC)	IPC 97-01 (-40°C / +125°C, 1cy/h)	500x
		1000x
Temperature Cycling on Board (TCoB NOKIA)	NOKIA Spec. (-40°C / +125°C, 2cy/h)	FF> 500 cycles
Drop Test	JESD22-B111	< 10% fails @ 20 drops
Drop Test	NOKIA Spec.	< 5% fails @ 30 drops

Qualification Vehicle:

9.25x8.80pkg
5.28x5.62 die
0.5 pitch
No UBM
122 Bumps

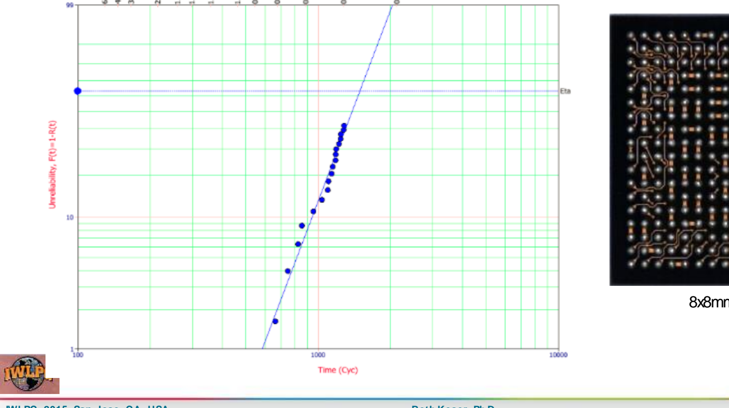
nanium

HAST = Highly Accelerated Stress Test

Reliability: DECA's M-Series BLR

Test Vehicle	Stack-up	Drop Results	Cycling Results
8X8 mm body 6 x 6 mm die 0.4 mm pitch BGA	7.5um PBO1, 7um Cu RDL, 9um PBO2, 9um UBM	First failure at 256 drops	First failure at 665 cycles

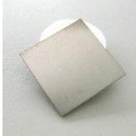
Temperature Cycle Results



8x8mm full array

Reliability: J-Devices PLP

Item	Design specifications
Package Size	12mmx12mm
Die size	6 mm x 6 mm
Ball pitch	0.50mm
Layers	2 Layers
Line/Space	20µm/20µm
Pad pitch	55/110µm(stagger)

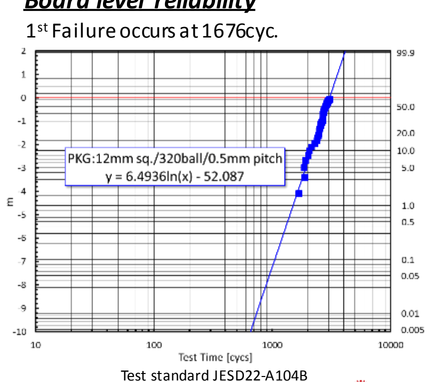


Package level reliability

Test Condition		# Failure
TC	JEDEC Level 1 -55/125°C 1000 cycle	0/231 pcs (3 Lots)
	JEDEC Level 3 -55/125°C 3000 cycle	0/231 pcs (3 Lots)
Unbiased HAST	JEDEC Level 1 130°C/85% 1000 hours	0/231 pcs (3 Lots)
HTS	JEDEC Level 3 150°C 3000 hours	0/231 pcs (3 Lots)

Board level reliability

1st Failure occurs at 1676cyc.



Test standard JESD22-A104B
(-40 degC to 125 degC)

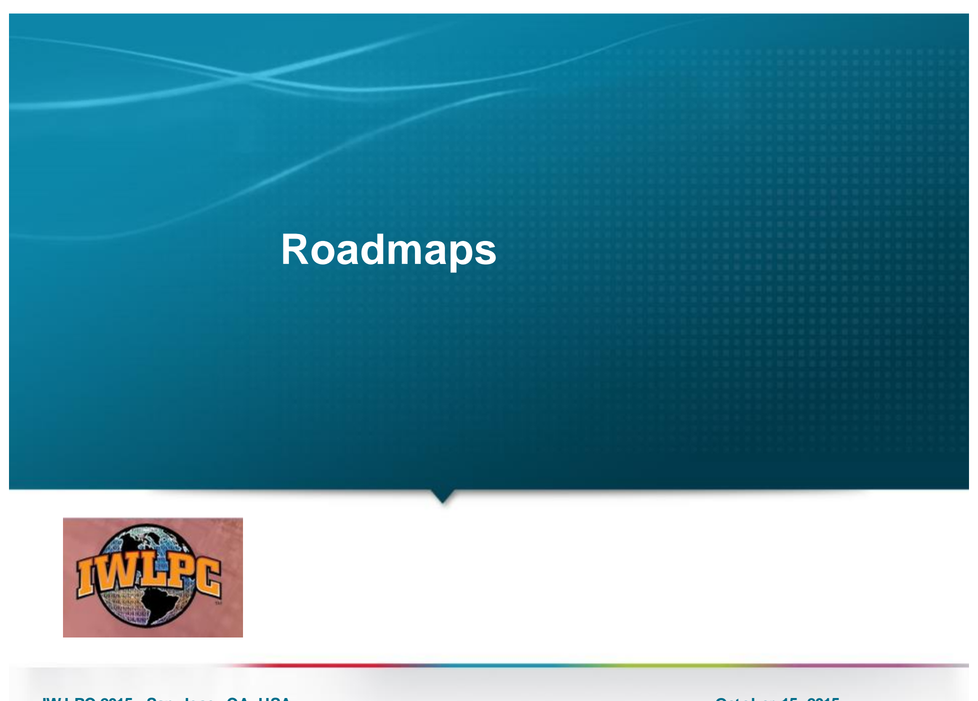
J DEVICES

Reliability: AT&S ECP®

Method	Specification	Result
Thermal cycling	-55°c / +150°C	1000 cycles passed (TC Grade 1)
Temperature / Humidity	85°C / 85%RH	1000 hours passed (TH Group A)
Board bending	5 mm/s	80k bends passed
Random vibration	3 g (rms) [5-500] Hz	30 min per axis passed
Shock	10k g @ 0,2ms	3 per direction passed
Reflow sensitivity	Pb-free profile (255°C)	30 cycles passed
HAST	110°C @ 85%RH @ 5VDC	264 hours passed
Drop test	1500g @ 0,5ms	10 drops passed (MS Group F)
High temperature storage	@ 125°C	1000 hours passed (TH Grade 2)
Moisture Sensitivity Level	Peak @ 260 °C	Minimum MSL 3

Reliability Summary

- FOWLP structures can pass MSL1
- Latest low cure dielectric materials can pass component level reliability with no issue (Thermal cycling condition B (TCB - 55ºC to 125ºC))
- Packages with conservative fan-out ratio (pkg area/die area) can pass board level reliability without UBM
- More board level reliability testing needed around small fan-out ratios, finer pitches, multi-layer RDL, and ball depopulations


Roadmaps
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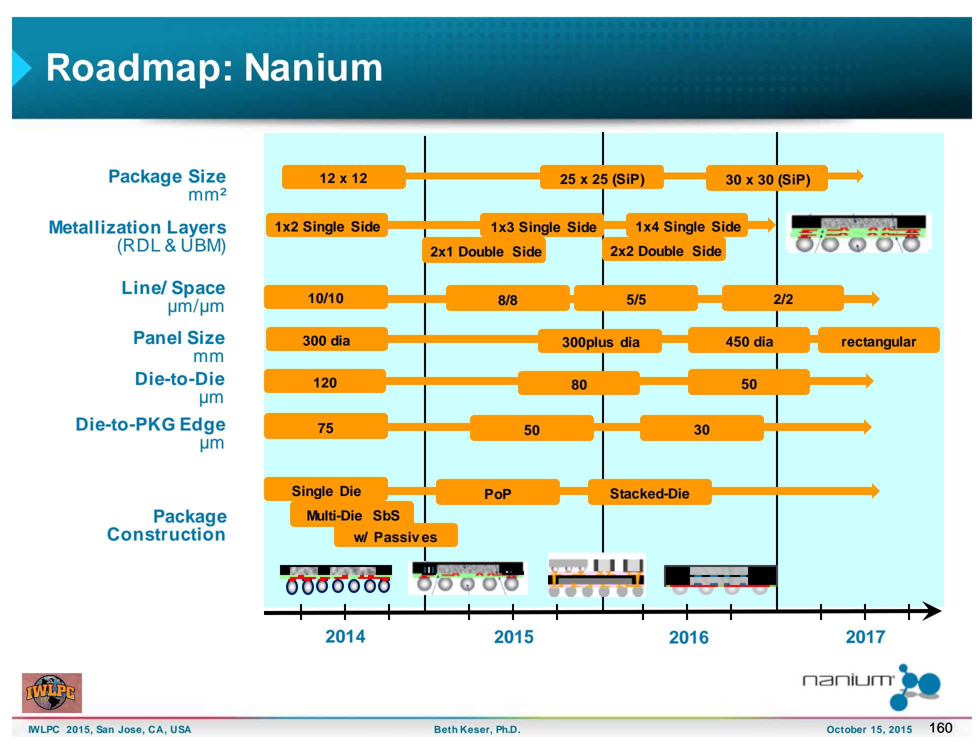
October 15, 2015


Roadmap: Nanium
Package Size
mm²
12 x 12
25 x 25 (SiP)
30 x 30 (SiP)
Metallization Layers
(RDL & UBM)
1x2 Single Side
1x3 Single Side
1x4 Single Side
2x1 Double Side
2x2 Double Side
Line/ Space
µm/µm
10/10
8/8
5/5
2/2
Panel Size
mm
300 dia
300plus dia
450 dia
rectangular
Die-to-Die
µm
120
80
50
Die-to-PKG Edge
µm
75
50
30
Package
Construction
Single Die
Multi-Die SbS
w/ Passives
PoP
Stacked-Die
2014
2015
2016
2017
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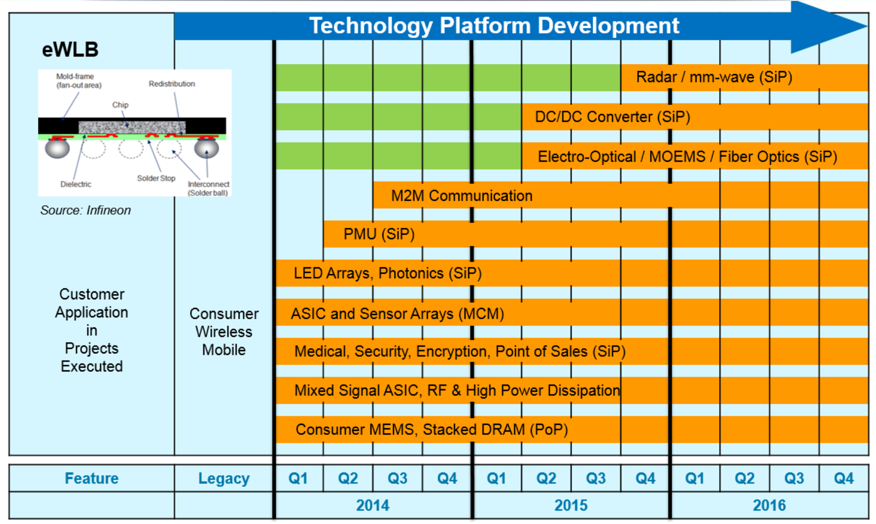
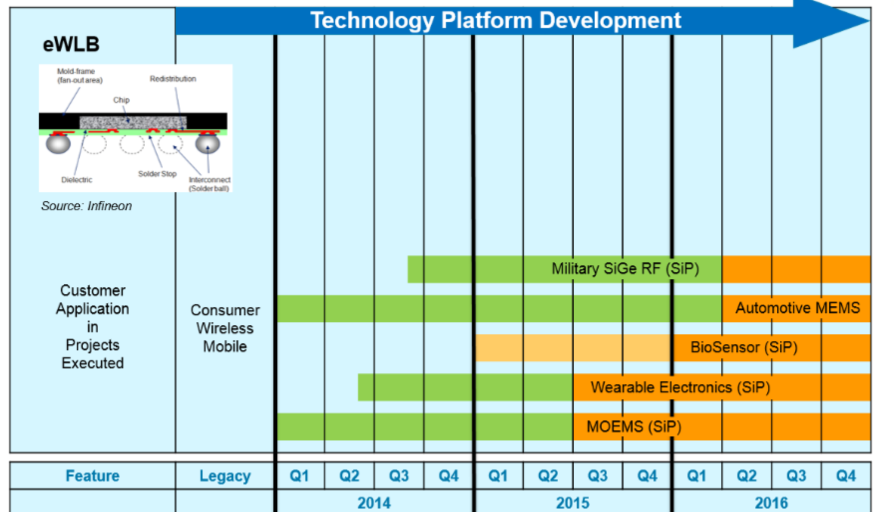
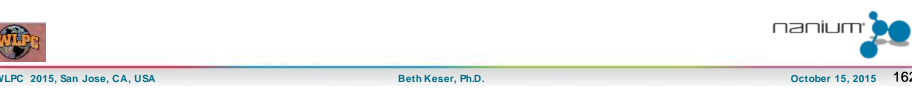
Markets & Applications

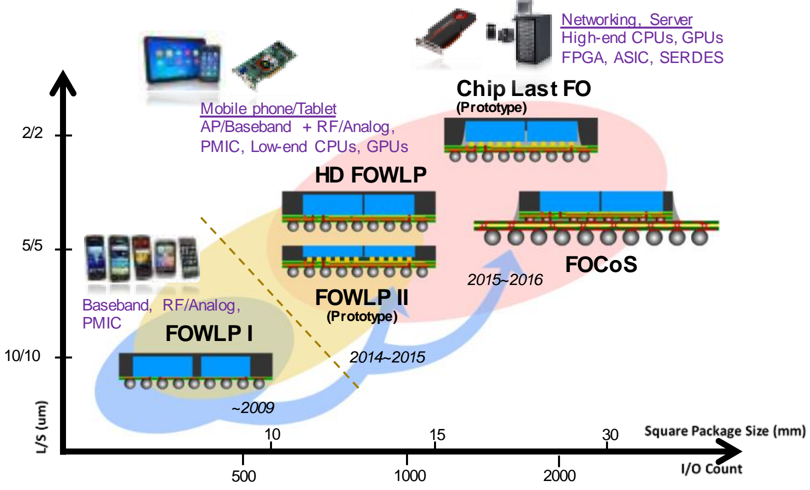


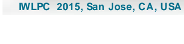
Markets & Applications

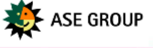




Roadmap: ASE

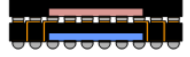


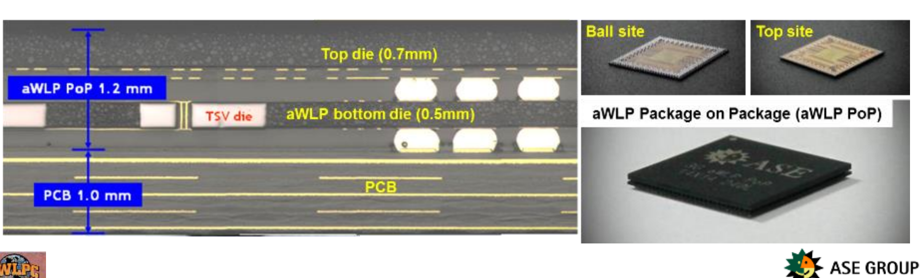


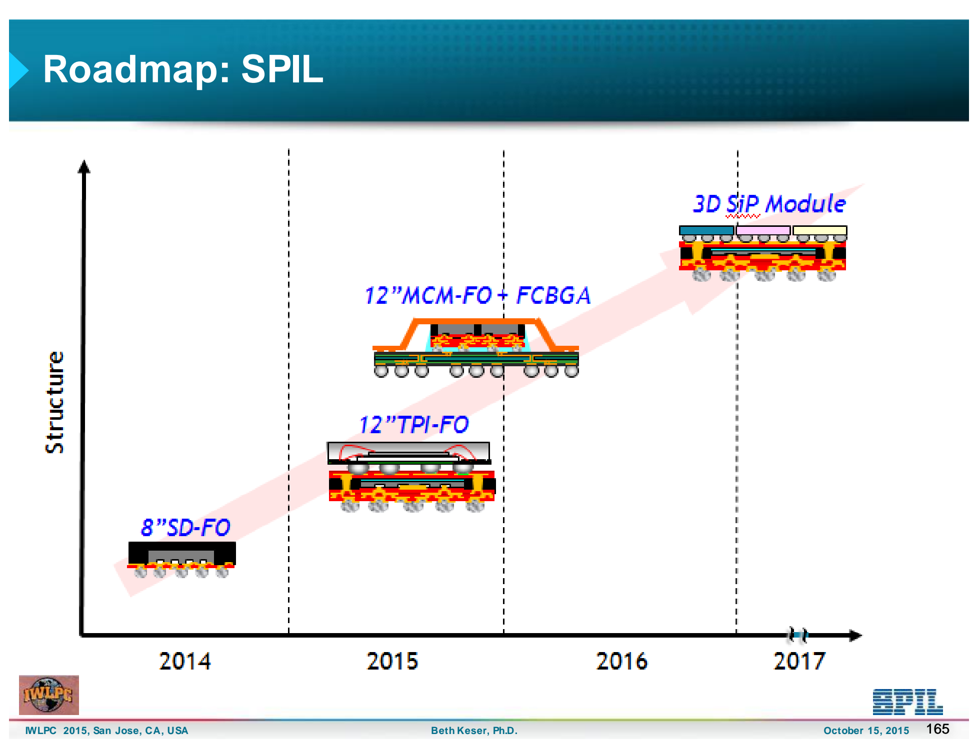


3D Double-sided

- **Two Approaches for 3D FOWLP**
  - Through Mold Laser Via
    - High level mold filler makes clean laser via difficult.
    - Rough sidew all challenges metallization of via.
- **Embedded TSV Die for 3D Feed through**
  - Embed small TSV die in mold compound as a 2D side-by-side aWLP for 3D interconnection.
  - Prototype device build up finished, and BLR evaluation done.







Roadmap: SPIL
Structure
3D SiP Module
12”MCM-FO + FCBGA
12”TPI-FO
8”SD-FO
2014
2015
2016
2017
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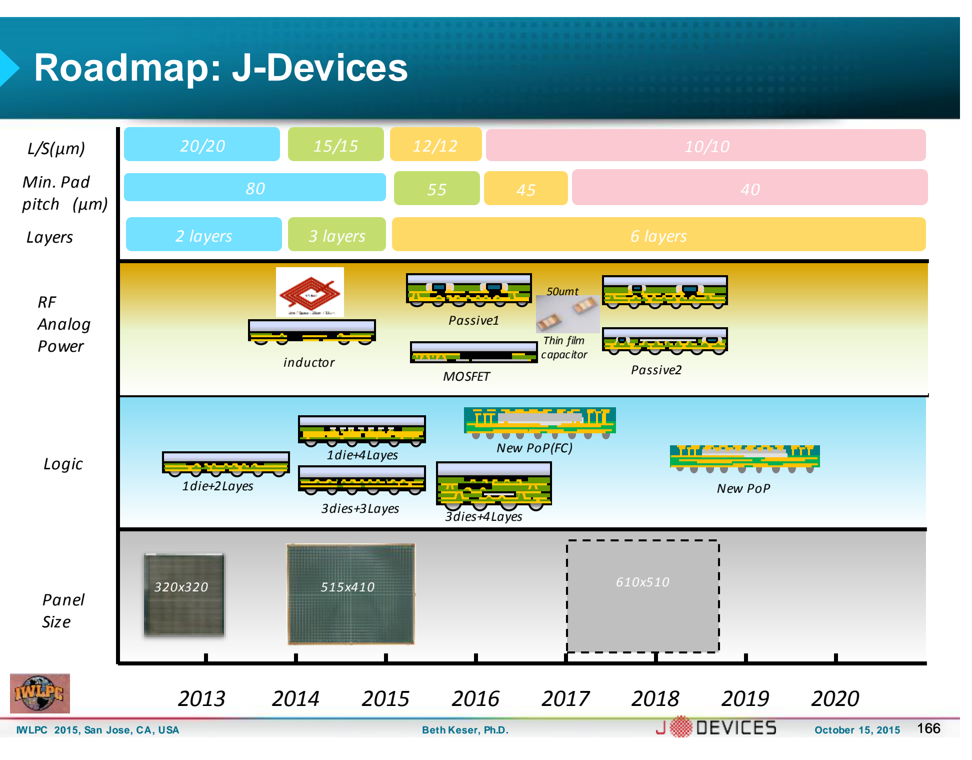

Roadmap: J-Devices
L/S(μm)
20/20
15/15
12/12
10/10
Min. Pad pitch (μm)
80
55
45
40
Layers
2 layers
3 layers
6 layers
RF Analog Power
inductor
Passive1
MOSFET
50umt
Thin film capacitor
Passive2
Logic
1die+2Layes
1die+4Layes
3dies+3Layes
New PoP(FC)
3dies+4Layes
New PoP
Panel Size
320x320
515x410
610x510
2013
2014
2015
2016
2017
2018
2019
2020
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J-DEVICES
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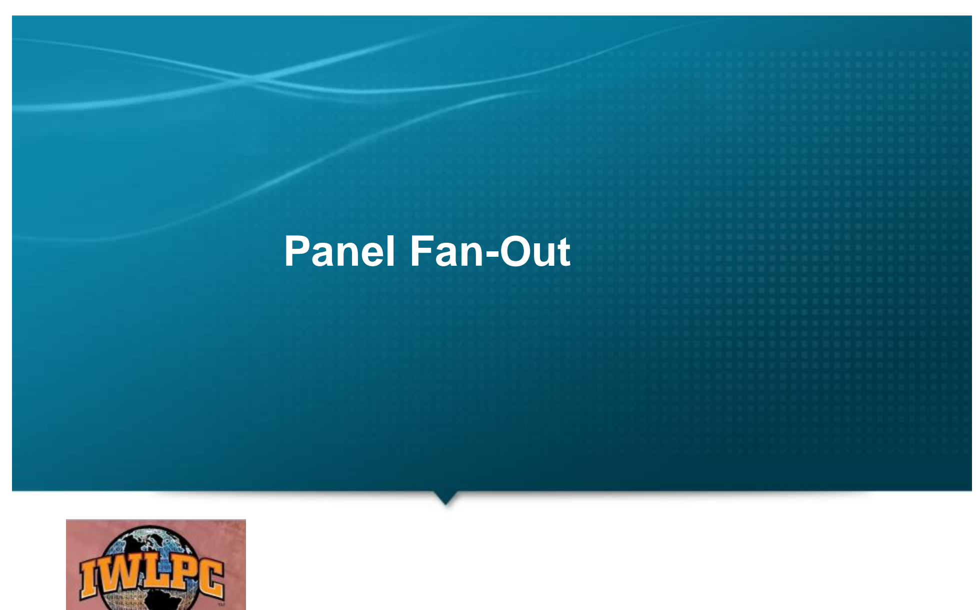
Panel Fan-Out
IWLPC
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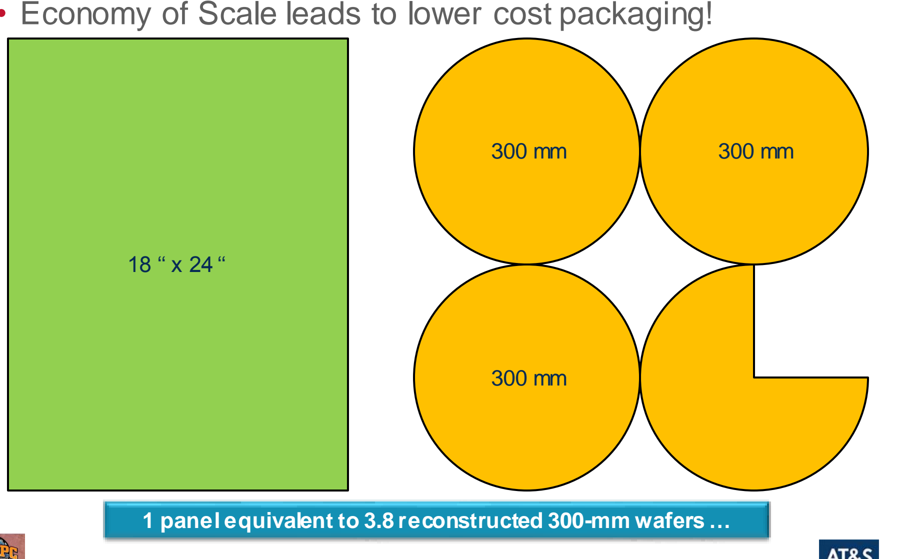
Panel FO Advantages
• Economy of Scale leads to lower cost packaging!
18 " x 24 "
300 mm
300 mm
300 mm
1 panel equivalent to 3.8 reconstructed 300-mm wafers …
AT&S
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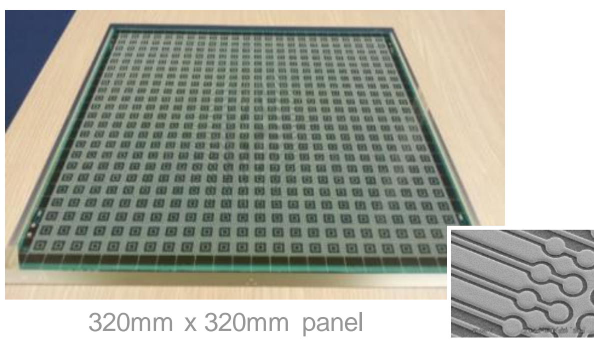
Panel FO Advantages

- Panel scale assembly
  - Large batch process
    - Packaging cost reduction can be realized.

Panel Level Package



320mm x 320mm panel

J DEVICES

Panel FOWLP

- Packages per Assembly Panel Considerations
  - 300mm wafer → 616 10mm x 10mm packages
  - 400mm X 500mm panel →1,911 10mmx10mm packages
- Organic technology vs. semiconductor technology
  - Equipment cost and throughput differences
  - Mold vs. laminate
  - Wafer like RDL process vs. build up layers
  - Minimum line and spacing differences

Palesko, IWLPC, 2014

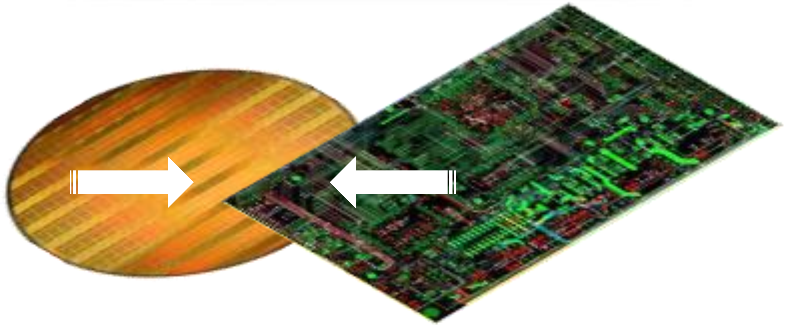
SavanSys
Supply Chain Cost Modeling

Panel FOWLP

- Panel technology has a cost advantage on large packages/dies
  - Large panel versus small wafer
- FOWLP has a design rule advantage due the use of semiconductor technology
  - Wafer processing equipment versus PCB panel processing equipment
- Both technologies are extremely sensitive to yield
  - Fabrication defects result in the scrap of the die and the package

Palesko, IWLPC, 2014

Panel: Intelligent Combination of WLP and PCB

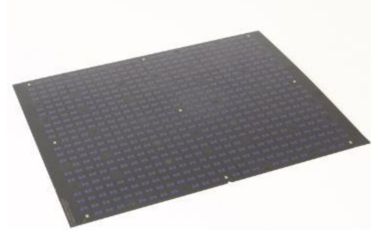


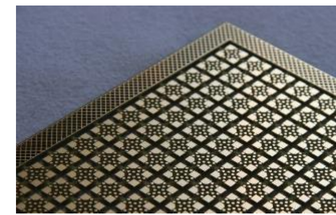
- Fusion of WLP/LCD/Substrate/PCB/Solar/Flex electronics
- Finer L/S from wafer level process
- Embedding die into substrates

Fraunhofer IZM

Panel Strategies

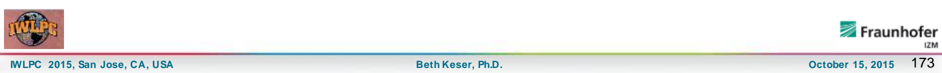
Panel-Size FO WLP | **PCB Embedding**





- Large-area molding 18" x 24"
- Through mold vias for 3D
- Interconnects using PCB materials & technology

- Use of new polymers / laminates
  - Thin layers (10 µm) for high density
- Need improved resolution for interconnects
  - 10 µm ➔ 5 µm ➔ 2 µm
- Need processes to reduce warpage



Fraunhofer IZM Panel Line

Placement ➔ Accuracy ➔ Molding ➔ Lamination ➔ Laser Drilling

Datacon evo/ ASM Siplace CA3

Mahr OMS 600/ IMPEX proX3

WL: Towa up to 8”
PL: APIC up to 18”x24” incl. 12” WL

Lauffer/ Bürkle

Siemens Microbeam/ Schmoll Picodrill with HYPER RAPID 50

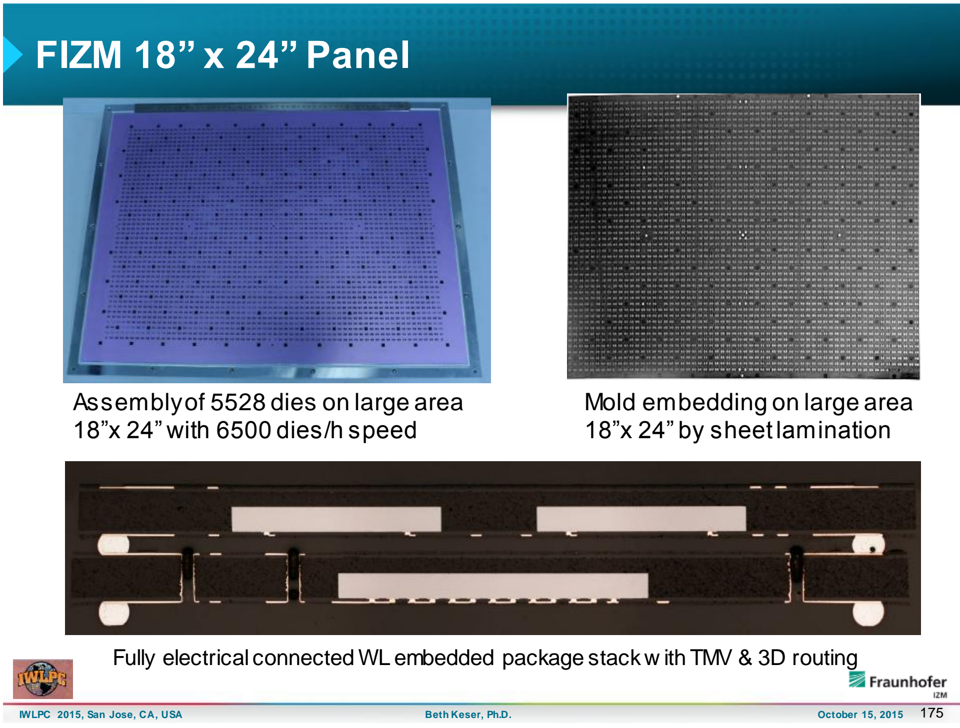
➔ Mech. Drilling ➔ Cu Plating ➔ Imaging ➔ Etching

Schmoll MX1

Ramgraber automatic plating line

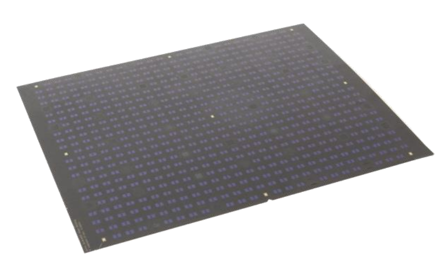
Orbotech Paragon Ultra 200

Schmid



FIZM Panel Molding

Equipment in Japan before shipment



First molded panel 18" x 24"

Large area compression molding:

- APIC Yamada
- Wafer Level: 300 mm up to 450 mm possible
- Panel Level: 18” x 24” (456 x 610 mm²)
- Lamination

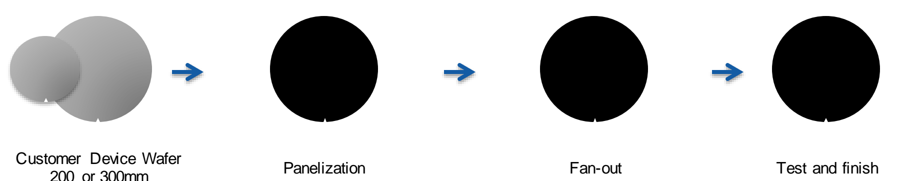
Fraunhofer IZM

Panel vs 300mm Round Trade-offs

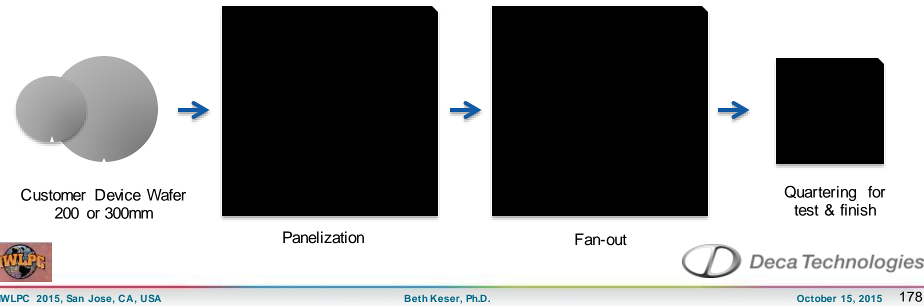
Attributes	300mm -- FO	Panel -- FO	Panel -- PCB
Pkg Cost	-	+	++
Capital	+	--	-
Capacity	-	+	+
Manufacturing Infrastructure	+	-	+
Yield	+	-	--
L/S	+	-	-
Die Prep	+	+	-
Application Space	High-end & Low-end	Low-end	Low-end

DECA's Large Panel Roadmap

Initial Production in 2015 – 300mm round

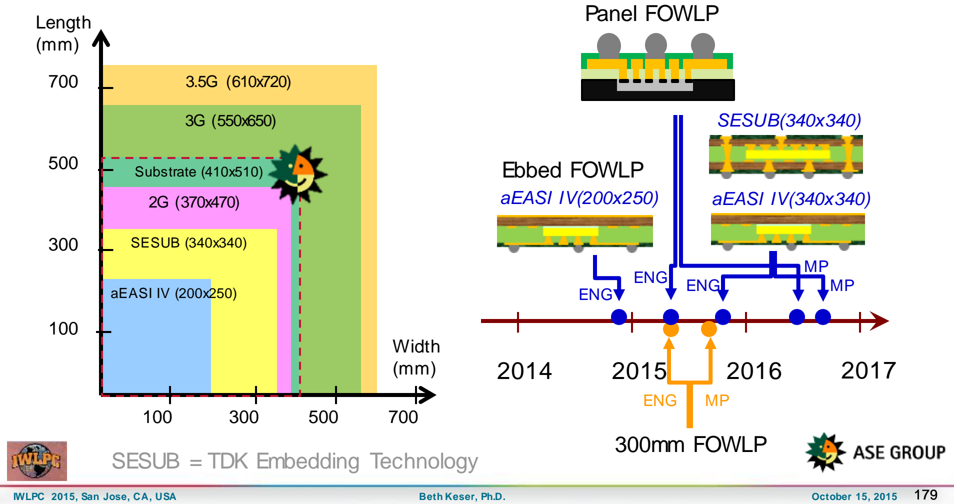


Future Capability in 2016 - Large Panel Format



ASE Panel Capability

- **Key Technology of Low Cost Fan-out Solution**
  - ASE equipment can meet current substrate panel size (410x510mm)

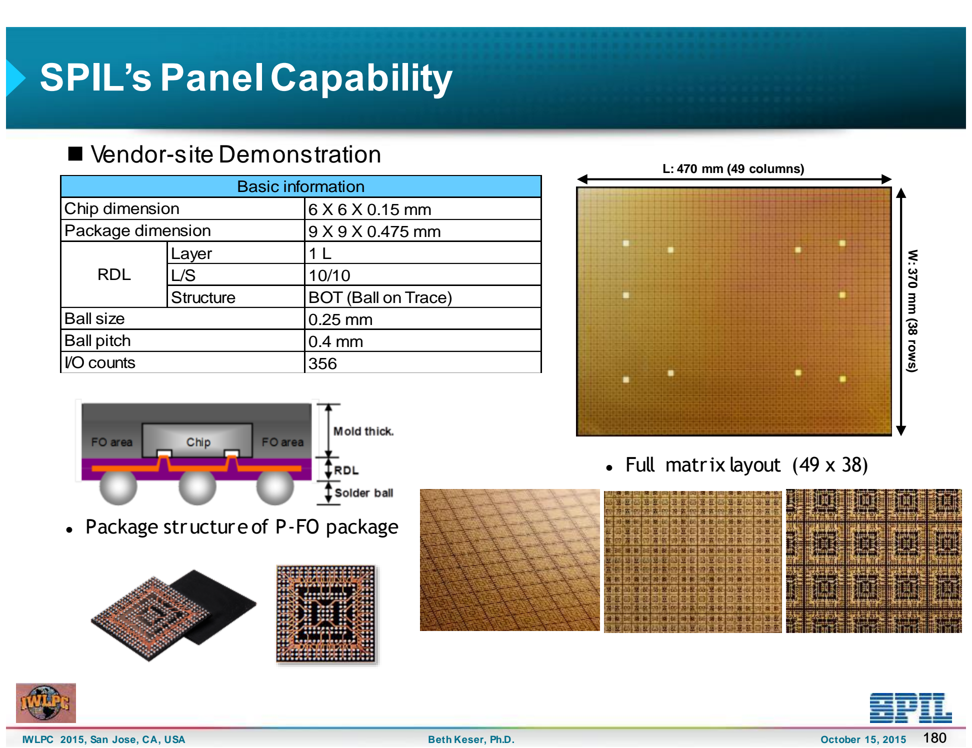


SESUB = TDK Embedding Technology

SPIL's Panel Capability

■ Vendor-site Demonstration

Basic information		
Chip dimension		6 X 6 X 0.15 mm
Package dimension		9 X 9 X 0.475 mm
RDL	Layer	1 L
	L/S	10/10
	Structure	BOT (Ball on Trace)
Ball size		0.25 mm
Ball pitch		0.4 mm
I/O counts		356



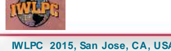
- Package structure of P-FO package
- Full matrix layout (49 x 38)

Low Cure Dielectric Panel Capability

- Slit coating is used for panel size substrate such as LCD, OLED.
  - Dielectric vendors need to test capability of slit coating
    - Demonstrate good uniformity on the panel substrate.

Sample	Test material
Substrate	Glass
Coating area	300mm × 300mm
Target thickness	12um
Thickness range at scan direction	<4%
Thickness range at nozzle direction	<4%

- Tune material for panel substrate
  - Test on glass
  - Test on molded die

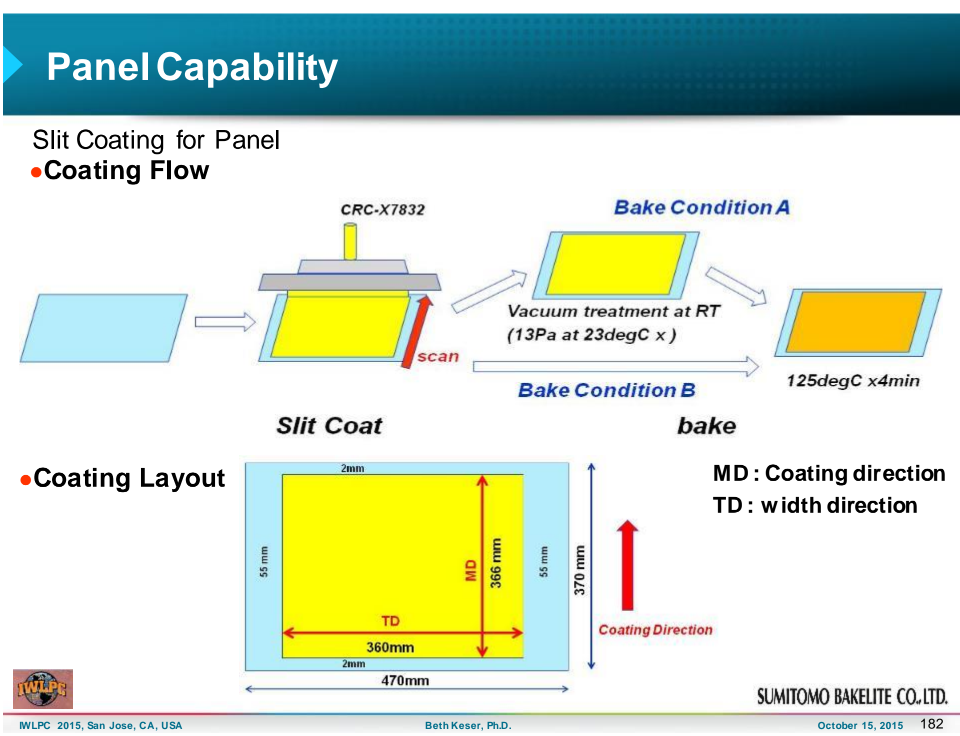


AsahiKASEI
ASAHI KASEI E-MATERIALS

Panel Capability

Slit Coating for Panel

- **Coating Flow**
- **Coating Layout**



SUMITOMO BAKELITE CO., LTD.

Panel Capability

Film Thickness and Uniformity

Bake Condition A
(vacuum treatment + 125degC x4min)

Bake Condition B
(125degC x4min)

Film Thickness(nm) vs. Measurement Point(mm) — charts with MD and TD series (y axis 10–20, x axis 0–400)

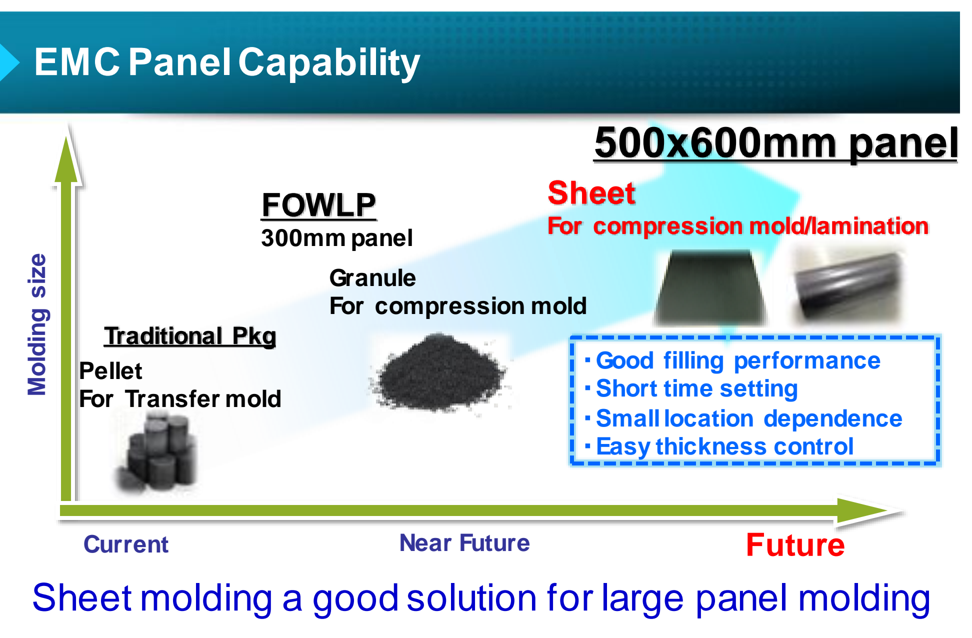
Bake Condition A:

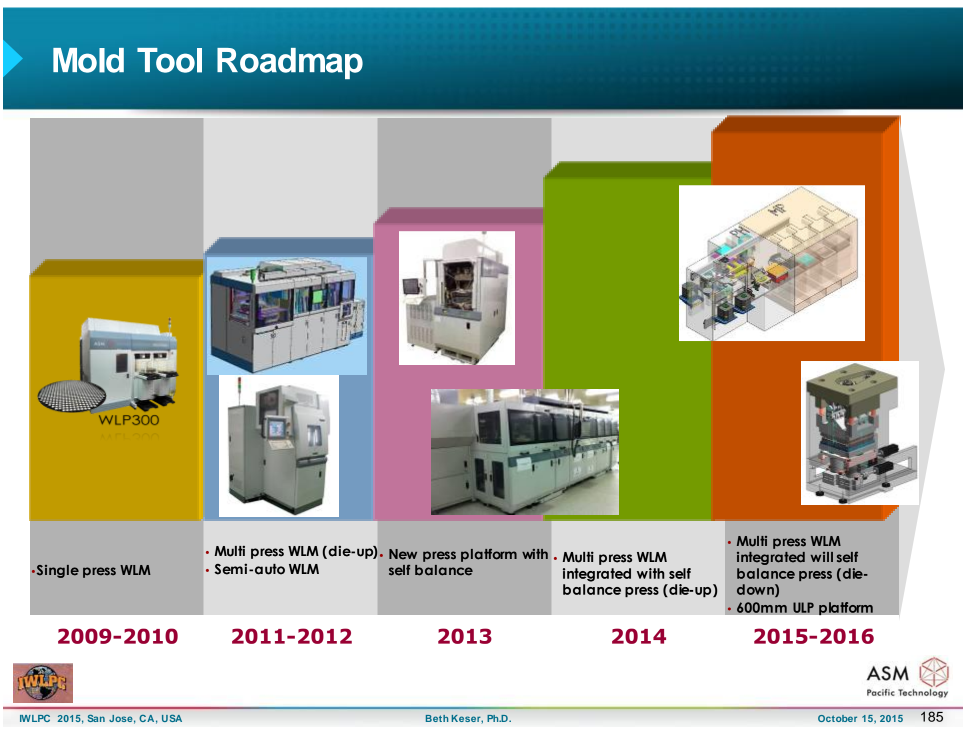
	Thickness (μm)	*Range (um)*
MD	*15.8*	*0.85*
TD	*15.7*	*0.84*

Bake Condition B:

	Thickness (μm)	*Range (um)*
MD	*16.0*	*0.96*
TD	*15.8*	*0.77*

✓ *Slit coater can be coated 15μm thickness film.*
✓ *Thickness uniformity in both conditions A and B was good.*




Mold Tool Roadmap
WLP300
•Single press WLM
• Multi press WLM (die-up)
• Semi-auto WLM
• New press platform with self balance
• Multi press WLM integrated with self balance press (die-up)
• Multi press WLM integrated will self balance press (die-down)
• 600mm ULP platform
2009-2010
2011-2012
2013
2014
2015-2016
ASM Pacific Technology
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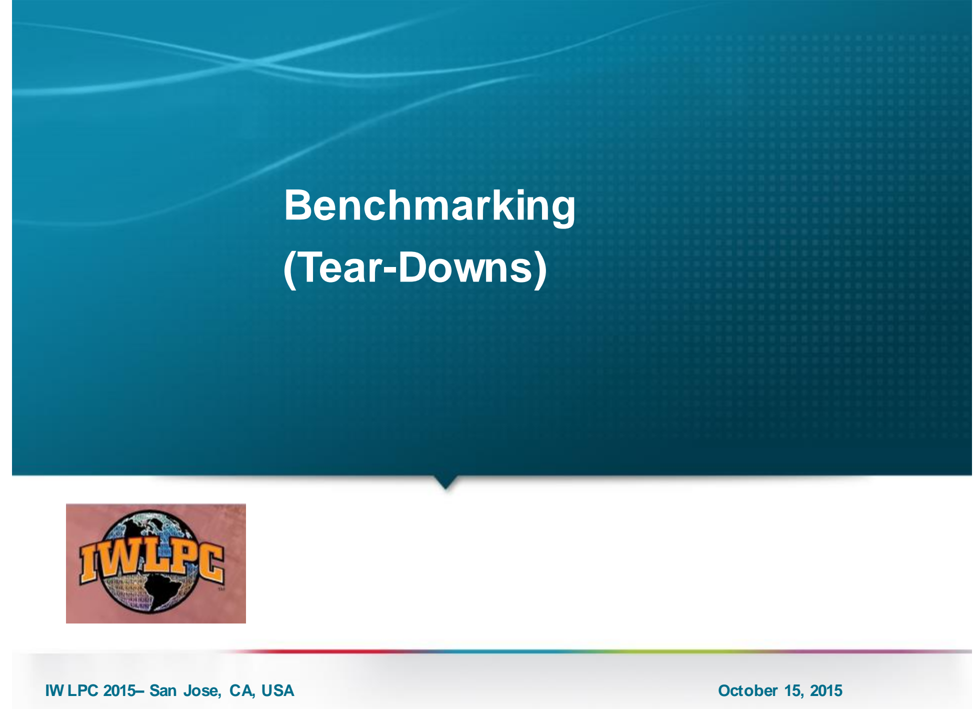
Benchmarking
(Tear-Downs)
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Device Manufacturers using FOWLP

- IMC/IFX
  - PMB5726-SMARTi LU
    - LTE Multimode RF Transceiver
    - 217 6.5x6.5x0.7 0.4P
    - 5.34mm x 5.16mm die
  - PMB8810
    - Single Chip Baseband, RF Transceiver, PM and FM radio
    - 217 8x8x0.7 0.5P
    - 5.44x5.21 die
  - PMB5712
    - Multimode RF Transceiver
    - 138 5.32x5.02 0.4P
    - 4.17x3.9 die
  - PMB9801
    - GSM/W-CDMA Baseband
    - 217 8x8 0.5P
    - 7.01x 6.99 die
  - PMB7900
    - GSM Baseband, RF Transceiver, Power Management, FM Radio
    - 184 8x8 0.5P
    - 4.6x4.25 die
- Marvell
  - PM820
    - Power Management w/Audio Codec
    - 133 6.3x4.7 0.4P
    - 3.89x2.44 and 1.79x1.79
- Spreadtrum
  - SC2712A
    - Power management
    - 217 8.1x6.9 0.4P
    - 5.7x2.5 die
  - SC8502
    - GSM / W-CDMA Baseband + RF Transceiver
    - 230 7.4x7.4 0.4P
    - 2.8x2.8 and 3.0x3.0 die
    - 2 metal layer RDL

Phones/Tablets with FOWLP (Samsung)

- Samsung Champ DUOS
  - The Champ DUOS is an entry-level GSM smart phone with a 2.6" color LCD with resistive touch screen and telescoping stylus.
- Samsung Galaxy S GT-i9000 UMTS
- Samsung Galaxy SII
  - Samsung's Galaxy SII comes in as a direct competitor to the iPhone lineup.
- Samsung Glide SGH-I927R
  - Released exclusively for Rogers Wireless in Canada, the Glide SGH-I927R is a new quad- band GSM / EDGE and tri-band W-CDMA / HSPA+ addition to Samsung's Galaxy series of mobile devices.
- Samsung Galaxy Nexus GSM/EDGE & W-CDMA/HSPA+ Touchscreen Smart Phone
  - This thin (9.0 mm) form-factor smartphone is quad-band GSM / EDGE and W-CDMA / HSPA+ (850/900/1700/1900/2100 MHz) compatible, with connectivity provided via WiFi
  - 802.11a/b/g/n, Bluetooth 3.0 + EDR, NFC, and USB 2.0.
- Samsung Galaxy S3 GT-I9300
  - The new S3 is touting a 1.4 GHz quad-core ARM 9 processor, an HD Super AMOLED 4.8" display protected by Corning's Gorilla Glass 2, an 8 MP rear camera and a forward facing 1.9 MP camera.
- Samsung Nexus S GT
  - Samsung's first NFC-capable smartphone was released in December 2010 and was co- developed with Google. The Nexus S is a high-end smartphone with features comparable to other premiere 3G smartphones and lacking only the latest trends of 4G/LTE connectivity and 3D screen.
- Samsung Captivate
  - One of a number of phones under the Galaxy umbrella. As one of the first phones to be powered by Samsung's 1 GHz "Hummingbird" Applications Processor.
- Samsung GT-P1000 Galaxy Tab UMTS Tablet
- Samsung Galaxy Tab 3 Lite (model SM-T110) tablet
  - 7.0-in. TFT-LCD display with WSVGA (1024 x 600) resolution, 16M colors, and a multitouch capacitive touchscreen. It runs the Android 4.2 "Jelly Bean".

Phones with FOWLP (Motorola)

- Motorola Droid Bionic XT875
  - Motorola released its first LTE phone, the Motorola Droid Bionic, in September 2011.
- Motorola Droid RAZR XT912
  - Introduced as a "Touch Tablet", the Droid RAZR mimics a small version of an Android tablet but has the features of a smart phone all in a surprisingly thin package.
  - The RAZR is advertised to support CDMA 800 & 1900 as w ell as LTE 700MHz. How ever, a deeper dive reveals more. Additionally, the RAZR uses Android 2.3.5 (Gingerbread) as w ell as a 4.3" Super AMLOED display w ith capacitive touchscreen. Other RAZR features include; 8MP camera, 1.3MP HD secondary camera, WiFi, Bluetooth, GPS, 4G mobile HotSpot capabilities.
- Motorola Droid 4 XT894
  - Android 2.3.5 "Gingerbread" smartphone that features a sliding QWERTY keyboard and is distributed by Verizon. It's advertised to support CDMA 850 and 1900 EV-DO as w ell as LTE 700 MHz

Phones with FOWLP (Nokia)

- Nokia C1
  - The C1 is a part of Nokia's economical C-Series of mobile handsets.
- Nokia 110 GSM/EDGE
- Nokia 1616-2c Dual-band GSM Phone
  - A basic, entry-level, bar-form mobile phone as part of the pre-paid device lineup for T-Mobile.
- Nokia X1-01

Phones/Tablets with FOWLP (Apple)

- Apple iPAD2 A1396 3G Tablet
- Apple iPhone4 A1332

Phones/Tablets with FOWLP (Other)

- LG Optimus 3D LG-P920
  - The LG Optimus 3D P920 is one of several mid-2011 smartphones available with an auto-stereoscopic GSM and multiple W-CDMA bands, the 3D display. Working over quad-band P920 uses EDGE and HSDPA for data while running the Android 2.2 OS.
- Huawei Ascend P1 (U9200)
  - Huawei Ascend P1 (also known as the U9200) is an Android smartphone supporting GSM, W-CDMA, and LTE bands. It has a 4.3-in. Super AMOLED display with a capacitive multi-touch screen overlay.
- Intel Xolo X900 AZ510
  - The Intel Xolo X900 AZ510 is a bar-format Android 2.3 ("Gingerbread") smartphone featuring a 4.03-in. 16M-color WSVGA TFT-LCD display (1024 x 600) and an integrated capacitive touchscreen overlaid with protective Corning Gorilla Glass. The X900 is designed to be compatible with quad-band GSM / EDGE (850 / 900 / 1800 / 1900 MHz) and W-CDMA / HSPA+ (850 / 900 / 1900 / 2100) cellular networks.
- K-Touch W806 Quad Band GSM EDGE WCSMA HSPA
- LG SU660 Optimus 2X UMTS
- Meizu MX 030
  - A smart phone supporting GSM / EDGE and W-CDMA / HSPA+. It's equipped with a 4-in 640x960 ASV TFT display overlaid with a multi-touch capacitive touchscreen.
- Meizu M9
- TCL Alcatel OT-C123
- Coolpad 8705
  - multimode, multiband smartphone that features a 4.7-in. TFT-LCD display with FWVGA (854 x 480) resolution, 16M colors, and a capacitive touchscreen. It runs the Android 4.3 "Jelly Bean".

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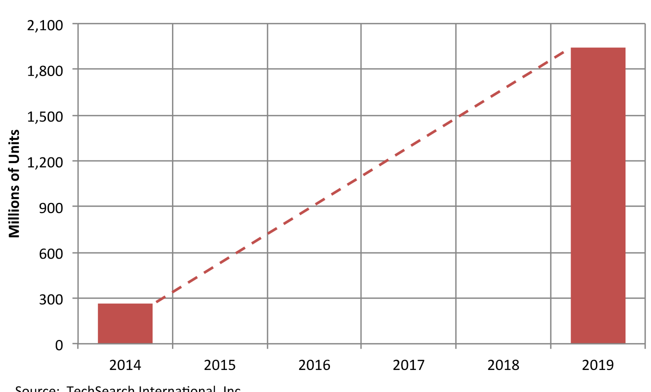
Projected Demand for FO-WLP



Source: TechSearch International, Inc.

- CAGR of 47%is projected 2014 to 2019
- WLP ~10% and FC ~15%

CAGR = Compound Annual Growth Rate

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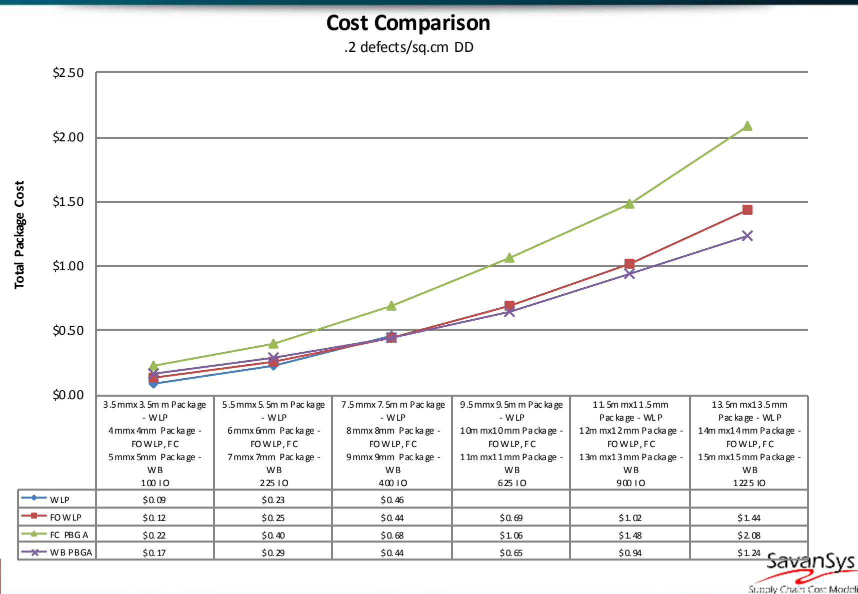
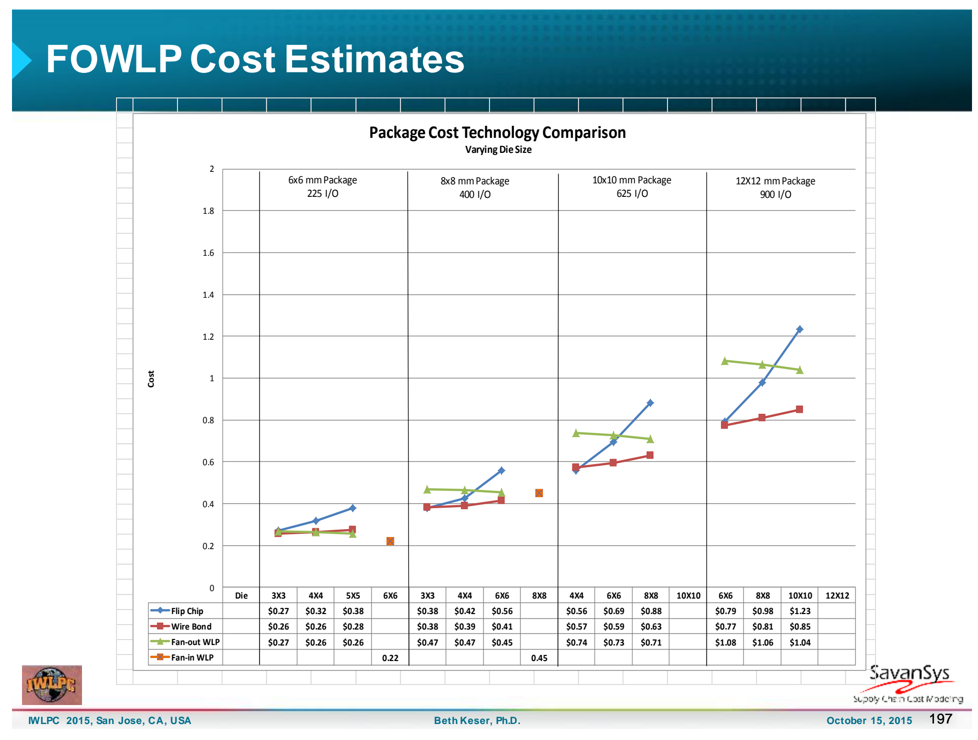
FOWLP Package Cost Estimates



	3.5mmx3.5mm Package - WLP 4mmx4mm Package - FOWLP, FC 5mmx5mm Package - WB 100 IO	5.5mmx5.5mm Package - WLP 6mmx6mm Package - FOWLP, FC 7mmx7mm Package - WB 225 IO	7.5mmx7.5mm Package - WLP 8mmx8mm Package - FOWLP, FC 9mmx9mm Package - WB 400 IO	9.5mmx9.5mm Package - WLP 10mmx10mm Package - FOWLP, FC 11mmx11mm Package - WB 625 IO	11.5mmx11.5mm Package - WLP 12mmx12mm Package - FOWLP, FC 13mmx13mm Package - WB 900 IO	13.5mmx13.5mm Package - WLP 14mmx14mm Package - FOWLP, FC 15mmx15mm Package - WB 1225 IO
WLP	$0.09	$0.23	$0.46			
FOWLP	$0.12	$0.25	$0.44	$0.69	$1.02	$1.44
FC PBGA	$0.22	$0.40	$0.68	$1.06	$1.48	$2.08
WB PBGA	$0.17	$0.29	$0.44	$0.65	$0.94	$1.24

FOWLP Cost Estimates

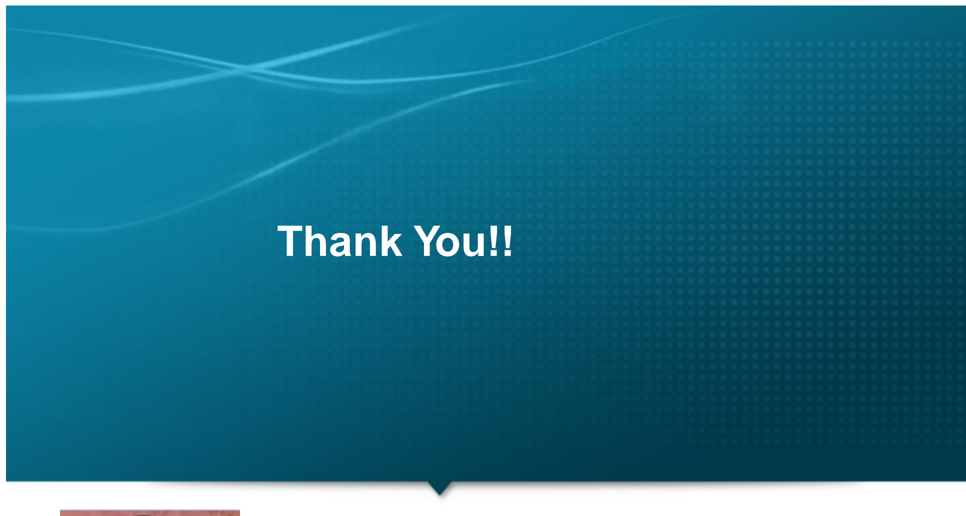


Die	3X3	4X4	5X5	6X6	3X3	4X4	6X6	8X8	4X4	6X6	8X8	10X10	6X6	8X8	10X10	12X12
Flip Chip	$0.27	$0.32	$0.38		$0.38	$0.42	$0.56		$0.56	$0.69	$0.88		$0.79	$0.98	$1.23	
Wire Bond	$0.26	$0.26	$0.28		$0.38	$0.39	$0.41		$0.57	$0.59	$0.63		$0.77	$0.81	$0.85	
Fan-out WLP	$0.27	$0.26	$0.26		$0.47	$0.47	$0.45		$0.74	$0.73	$0.71		$1.08	$1.06	$1.04	
Fan-in WLP				0.22				0.45								

SavanSys
Supply Chain Cost Modeling

Summary

- Multiple application and device drivers for fan-out and embedded packaging technologies
  - Larger WLP
  - Coarser pitch WLP
  - Module
  - SiP
  - PoP
- Multiple fan-out and embedded technologies offered
  - eWLB dominates HVM
- Selection will depend on time-to-market, integration need, yield requirement, and supply chain requirement



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- Garrou, "IFTLE 213 What's New in Permanent Polymer Dielectrics: Dow, HD Micro, Zeon," Solid State Technology, Insights From the Leading Edge, October 2014.