Acronyms and Definitions

ACA – Anisotropic Conductive Adhesive ACF – Anisotropic Conductive Film APWB – Advanced Printed Wiring Board ASIC – Application Specific Integrated Circuit

BBUL – Bumpless Build Up Layer **BCB** – Benzene Cyclobutene (Cyclotene)

BCB – Belizelle Cyclobulelle (Cyclob

BGA – Ball Grid Array

BUT – Build Up Technology

C-4 – Controlled Collapse Chip Connection
C-4NP – C-4 New Process
CAD – Computer Aided Design
C & W – Chip and Wire
CBGA – Ceramic Ball Grid Array
CC – Chip Carrier
CMOS – Complimentary Metal Oxide Semiconductor
CMP – Chemical Mechanical Polishing
COB – Chip On Board
CSP – Chip Scale Package

DCA – Direct Chip Attach DIP – Dual Inline Package DRAM – Dynamic Random Access Memory

ECBU – Embedded Chip Build Up **ESD** – Electro Static Discharge

FC – Flip Chip FCA – Flip Chip Assembly FCM – Few Chip Module FCOB – Flip Chip On Board FCIP – Flip Chip In Package FP – Flat Pack FQFP – Fine Pitch Quad Flat Pack

GaAs - Gallium Arsenide

HC – Hybrid Circuit HDI – High Density Interconnect HDI-PWB – High Density Interconnect Printed Wiring Board HIC – Hybrid Integrated Circuit HTCC – High Temperature Cofired Ceramic

I/O – Input/Output

IC - Integrated Circuit

ICA - Isotropic Conductive Adhesive

ILB – Inner Lead Bond

ICF – Isotropic Conductive Film

KGB - Known Good Board

KGD - Known Good Die

LCCC – Leadless Ceramic Chip Carrier

LCD – Liquid Crystal Display

LCP - Liquid Crystal Polymer

LDCC - Leaded Ceramic Chip Carrier

LID – Leadless Inverted Device

LSI – Large Scale Integration

LTCC – Large Scale Integration

Micro BGA (µBGA) – Micro Ball Grid Array

MCM – Multichip Module

MCM-C – Multichip Module-Ceramic (Thick Film or Cofired Ceramic)

MCM-D – Multichip Module-Deposited (Thin Film)

MCM-L – Multichip Module-Laminate (Lamination)

MCP – Multichip Package

MEMS – Micro Electro Mechanical System

MIB – Multilayer Interconnect Board

MIC – Microwave Integrated Circuit

MLB – Multilayer Board

MLC - Multilayer Ceramic

MMIC - Monolithic Microwave Integrated Circuit

MPM – Multi Package Module

MOS – Metal Oxide Semiconductor

MQFP - Metric Quad Flat Pack

MSI - Medium Scale Integration

MTBF – Mean Time Between Failures

MTTF – Mean Time To Failure

NCA – Non-Conductive Adhesive

NCF – Non-Conductive Film

OLB - Outer Lead Bond

PBGA – Plastic Ball Grid Array PCA – Printed Circuit Assembly PE – Packaging Efficiency **PGA** – Pin Grid Array PI – Polyimide PLCC – Plastic Leaded Chip Carrier **PoP** – Package on Package **PPM** – Parts Per Million **POFP** – Plastic Ouad Flat Pack **PTF** – Polymer Thick Film **PTH** – Plated Through Hole PCB - Printed Circuit Board **PWA** – Printed Wire Assembly **PWB** – Printed Wiring Board **QFP** – Quad Flat Pack **QFN** – Quad Flat Pack No Leads **RAM** – Random Access Memory ROM – Read Only Memory **SAW** – Surface Acoustic Wave **SBB** – Stud Ball Bump **SCP** – Single Chip Packaging SEM – Scanning Electron Microscope SEM – Standard Electronic Module Si – Silicon SiGe – Silicon Germanium **SIP** – Single Inline Package SiP – System in Package **SLC** – Sequential Laminar Circuitry SoP – System on Package **SMA** – Surface Mount Assembly **SMD** – Surface Mount Device **SMT** – Surface Mount Technology **SOC** – System on Chip **SOIC** – Small Outline Integrated Circuit **SON** – Small Outline No Leads **SOP** – Small Outline Package SOT – Small Outline Transistor **SSI** – Small Scale Integration **TAB** – Tape Automated Bonding TBGA – Tape Ball Grid Array

TCE – Temperature Coefficient of Expansion

TC – Thermocompression (bonding)

Tg – Glass Transition Temperature

TS – Thermosonic (bonding)

264 Integrated Circuit Packaging, Assembly and Interconnections

ULSI – Ultra Large Scale Integration US – Ultrasonic (bonding)

VLSI – Very Large Scale Integration

WL-CSP – Wafer Level Chip Scale Package WLP – Wafer Level Packaging

Compiled by W.J. Greig

Microelectronics Glossary

- A
- ACTIVE CIRCUIT AREA All areas on the die from outside edge of the bond pads inward.

ACTIVE DEVICE – An electronic device, a bare die or a packaged component a diode, transistor or integrated circuit.

- ADHESION The sticking together of two different materials.
- ALLOY A solution of two or more metals.
- ALUMINA Aluminum oxide (AI₂O₃). Ceramic substrates used in microelectronic applications are made of formulations that are primarily (92%, 96% and 99%+) alumina.
- AMBIENT The temperature and/or pressure and/or humidity of the atmosphere surrounding a device.
- ANISOTROPIC Single directional material property, as opposed to isotropic with material properties the same in all directions. For example, an anisotropic conductive adhesive is conductive in the z-direction only.
- ANNEALING Slow heating and/or cooling of a material to relieve stresses and thereby stabilize the material properties.
- ANODIZING An electro-chemical process for oxidizing metals, most often aluminum.
- APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) A custom designed, not off the shelf, IC intended for a distinct application.
- AREA ARRAY Refers to the configuration of the I/O pads on a device or package. Pads are arranged in an x-y grid format with pins, solder balls or columns for attachment.
- ARTWORK The circuit pattern, typically a drawing at 10X, from which screens or photomasks can be fabricated using photographic reduction.
- ASSEMBLY The attachment of components, packaged or bare die active and passives, to a package, substrate or board. Also refers to a substrate or board to which components have been attached.
- ASSEMBLY DRAWING A drawing showing where each component is to be attached onto a substrate or board and the assembly sequence of the parts.

B

- BACK END In semiconductor manufacturing the point at which all wafer processing has been completed and testing, assembly and packaging begins.
- BAKE Subjecting a part, package, board, substrate or an assembly to an elevated temperature. Used primarily to drive off moisture or contaminants, e.g. organics, or assess quality of surface finish, e.g. blisters in plating. Used to react compo-

nents with in a formulation, e.g. photoresist or a polymer to pre-cure or fully cure.

- BALL BOND In chip and wire assembly, a bond formed with a capillary tool where the end of the wire has first been shaped into a ball.
- BALL BONDING A wire bonding technique in which the wire is inserted into a capillary tool and by heating a ball is first formed at the end of a wire. The bond is formed between the ball and a metal pad by heating and application of pressure by the bonding tool (capillary).
- BALL GRID ARRAY (BGA) A packaging technology in which a device's I/O pads are arranged as an array of conducting pads on the base of the package. Small balls of solder are attached to each conducting pad.
- BALL BUMPING The process of forming or placing bumps on packages or bare die, in wafer format or singulated, using a wire ball bonder.
- BARE DIE An unpackaged transistor, diode or integrated circuit.
- BISBENZOCYCLOBUTANE (BCB) High purity polymer resins formulated as high-solids, low viscosity solutions developed for specifically for microelectronic applications including use as an inner layer dielectic in multilevel metallization structures.
- BERYLLIA Beryllium Oxide (BeO). A ceramic used to fabricate substrates having very high thermal conductivity.
- BINDERS Materials, usually organic, added to thick film paste to enhance the flow properties during printing and firing. Binders are also added to ceramics as sintering aids.
- BLEED OUT Die attach adhesives will leak out from under the die before it is cured. This "leakage" is called "bleed". Since wire bonds will not stick in areas where bleed has occurred it is important that bleed not exceed a few mils. Bleeding can be controlled by formulation (filler particle size, resin/hardener selection) and process (cure temperature, out time). In addition material will bleed differently on different surfaces (silver, Nickel, palladium, solder mask, polyimide).
- BOARD Typically refers to a printed wiring board (PWB) or a printed circuit board (PCB).
- BOND A permanent attachment to form an electrical or mechanical interconnection.
- BONDABILITY Those conditions of surface condition, technique and materials that enhance attachment of two materials together.
- BOND AREA The area within which the attachment is to be accomplished. On an active device or package/substrate it is referred to as the bond pad.
- BOND DEFORMATION In wire bonding it is the change in dimensions of the wire at the attachment point produced by the bonding tool and the application of temperature, a mechanical force and/or ultrasonic energy. The deformation is usually measured as a percentage of deformation to original wire diameter in units of wire diameter.
- BONDING ENVELOPE/BONDING WINDOW The range of bonder machine parameters/settings over which acceptable bonds may be obtained.

- BOND INTERFACE In the case of a wire bond it is the wire to the bonding pad surface. In the case of adhesive die attach it is the die to adhesive surface and the adhesive to substrate surface.
- BOND LIFT-OFF The failure mode where a bonded wire separates from the bonding surface.
- BONDING SCHEDULE The various parameter settings on a bonder for wire bonding, for example, the settings for temperature, applied force, bonding time and power.
- BOND STRENGTH In wire bonding, the pull force at failure of a bonded wire when subjected to a destructive wire pull test or bond shear. Several failure modes are possible including bond lifts and wire breaks. The bond strength is measured in grams of force.
- BONDING WIRE Fine gold, aluminum or copper wire used to make electrical connection between the active device bond pads and the package or substrate pads.
- BOW The deviation from flatness of a package/substrate or board. Same as warpage and camber.
- BUMPING PROCESS The deposition of bumps, typically solder or other conducting material onto device bond pads to be used for the attachment medium to a package or substrate. Most commonly performed while devices are in wafer format. Typically involves deposition and patterning of an under bump metallization followed by the bump deposition by electroplating or stencil printing of solder paste. See Wafer Bumping. For CSP and BGA, balls are mechanically placed using specially designed placement equipment. Bumping is also accomplished using wire bonding. See Stud Bumping.
- BURN-IN The process of electrically stressing a device at an elevated temperature for an adequate period of time intended to cause rapid failure of marginal devices.

С

CAMBER - The amount of bow or warpage in a board or substrate. See BOW.

- CAPILLARY In wire bonding a tool used to guide wire and to apply pressure to form a bond between the wire and a metallized pad on a device, package or substrate.
- CAPILLARY ACTION The action by which the surface of a liquid in contact with walls of a capillary tube or between two closely spaced plates is drawn into the tube or between the plates by a wicking action. An example of capillary action is in the flip chip assembly, the underfill is dispensed next to the die and the material is pulled into the gap by the force of capillary action.
- CENTRIFUGE A method of testing circuits and packages by spinning at high speed. Places high "G" loads (a centrifugal force) on IC's and bonds to evaluate mechanical robustness).
- CERAMIC An inorganic material that is a non-conductor of electricity. Examples are alumina (Al₂O₃), beryllia (BeO), aluminum nitride (AlN) steatite, or forsterite. All have high temperature melting points. Ceramics are used extensively in microelectronics manufacturing as packages or substrates.

- CERDIP A ceramic dual in-line package.
- CERMET A mixture of glass and/or ceramic, it has come to mean the general class of high resistivity thick film resistors and dielectrics paste materials that are fired at temperatures above 500°C.
- CHAMFER A corner or edge of a substrate or board that is broken or shaped to eliminate a sharp edge or to identify a desired part's orientation.
- CHEMICAL VAPOR DEPOSITION (CVD) Deposition by reduction or decomposition of a material to vapor onto a substrate. Generally accomplished in a plasma system.
- CHIP (1) Active Unpackaged bare die, e.g. a diode, transistor, or IC. (2) Passive – A discrete capacitor, resistor, inductor.
- CHIP CARRIER A type of package or substrate, used to enable electrical testing and provide mechanical and environmental protection to active devices. See also PACKAGE.
- CHIP AND WIRE ASSEMBLY (C&W) Wire bonding bare die to a package, substrate or board using Au, Al or Cu wire for electrical interconnection.
- CHIP ON BOARD (COB) Assembly of bare die wire bonded to an organic substrate or printed wiring board. As a packaging option COB is classified as a "packageless packaging" approach that enhances reliability with the elimination of the package. The bare die may be glob topped with an organic coating to protect the wire bonds and die.
- CHIP SCALE PACKAGING (CSP) A package format where the package area is no more than 1.2 times the area of the die.
- "CHIPS FIRST" PACKAGING A packaging technology where all die are first attached to a substrate or organic film and interconnect circuitry to individual die and between die is subsequently fabricated into a finished single or multichip package. There is no wire bonding, flip chip or TAB assembly required.
- "CHIPS SECOND" PACKAGING A packaging technology in which all die are assembled using chip & wire, flip chip or TAB, to a pre-fabricate package or substrate containing the necessary interconnect circuitry.
- CHLORINATED SOLVENTS Hydrocarbon liquids containing chlorine. Most commonly used in cleaning processes.
- CIRCUIT A conductor interconnect for a number of elements and/or devices designed to perform a desired electrical function.
- CLAMPING FORCE In wire bonding, the force applied to the wire by the bonding tool to affect a bond.
- CLADDING A method of applying a metal foil to a substrate. See COPPER CLADDING.
- CLEAN ROOM An area in which a high degree of cleanliness is realized and maintained by controlling the generation and distribution of particulate matter inside the room. Cleanliness is achieved by air filtering systems in a controlled environment, i.e., temperature and humidity. Clean rooms are classified based on the allowable number and size of particles of per cubic feet. For example, a Class 100 clean room refers to a room in which no more than 100 particles greater than 0.5 micrometers in diameter are present.
- COEFFICIENT OF THERMAL EXPANSION (CTE) How much a material grows when heated and shrinks when cooled. The unit of measure is parts per million

(ppm) per degree centigrade. The CTE differences (CTE mismatch) among the materials in a semiconductor package will cause stress as the part is exposed to temperature changes in its working life. In most cases, it is important for an epoxy connecting two materials to have a CTE that falls between the CTE's of the materials being joined.

COFIRING - Firing of two or more materials at the same time.

- COLD SOLDER JOINT A solder connection that was made at too low a temperature. The joint usually appears rough and dull and is generally unreliable.
- COMPATIBLE Refers to materials that can be used together with minimum adverse reaction, e.g. the bonding wire and the die or package metal bond pad.
- COMPONENT A packaged active or discrete passive device.
- CONDUCTIVE ADHESIVE: An adhesive material (usually epoxy) that has metal powder (usually silver or gold) added to increase electrical conductivity. Same as conductive epoxy.
- CONDUCTIVE EPOXY A polymer resin that has been made conductive by the addition of a metal powder, usually silver or gold.
- CONDUCTIVITY The ability of a material to conduct electricity.
- CONDUCTOR A class of materials that conduct electricity.
- CONDUCTOR FILM a metal trace deposited by thick or thin process and patterned on a substrate.
- CONDUCTOR SPACING The distance between adjacent conductor traces. Measured from the outside edge one trace to the inside edge of another.
- CONDUCTOR WIDTH A measurement of a conductor trace from edge to edge.
- CONDUCTOR THICKNESS The height of a conductor trace, measured from the substrate to the top surface of the conductor.
- CONFORMAL COATING A thin nonconductive coating that may be organic (polyimide, for example) or inorganic (glass) whose purpose is to protect circuitry and circuit elements. Conformal coatings are typically non-planarizing.
- CONTACT PRINTING (1) A method of screen printing whereby the screen is in contact with the substrate to be printed and there is zero snap-off. (2) In the photolithography image transfer process where the photomask and resist coated substrate are in intimate contact.
- CONTACT RESISTANCE A measure of the quality of an electrical connection between two contact pads, e.g., a wire bond. Contact resistance is measured in milli-ohms.
- CONTINUOUS BELT FURNACE A furnace that uses a moving belt to transport parts through the furnace.
- CONTROLLED COLLAPSE Minimization of the amount of decrease in bump size, e.g. solder ball diameter, following reflow attachment.
- COPPER CLADDING A sheet of Cu foil bonded to an organic core to form the base material for a printed wiring board.
- CRAZING Fine cracks found in brittle materials.
- CRITICAL DIMENSION In microelectronics packaging, the smallest feature size to be defined in patterned circuitry.
- CROSSOVER Transverse crossing of a metal by another metal without electrical contact and achieved by the deposition of an insulating layer between the conductors at the area of crossing.

- CROSSTALK Signals from one conductor trace leaking into another nearby conductor because of capacitive or inductive coupling or both.
- CURE A non-specific term that is widely used to mean the solidification of a polymer. Curing can be accomplished by applying heat or UV light.
- CURE TIME The time required to fully harden an organic material, e.g., an epoxy, under a defined set of conditions.
- CUSTOM CIRCUITS A circuit designed for a single specific application. See Application Specific Integrated Circuit.
- CYCLIC STRESS A method of testing circuits by subjecting them to various cycles of temperature, or power, humidity or voltage. A method of doing accelerated testing.
- CYCLOTENE®TM The commercially available version of BCB, the insulating polymer derived from bisbenzocyclobutane.

D

- DEFECT An anomaly that is in non-conformance with normally accepted characteristics.
- DEFINITION The sharpness of a deposited pattern, or the exactness with which a feature is patterned with respect to the intended design.
- DEGRADATION A debilitating change in a material characteristic or a device performance.
- DENSITY In packaging: Refers to the number of components on a circuit or board or the amount of conductor circuitry on a device package, a substrate or board.
- DEVICE A bare die (an element) or a packaged component.
- DEWETTING A condition that results when molten solder has coated a surface and upon cooling recedes leaving areas of uncovered base material.
- DICE Plural of die.
- DIE An unpackaged semiconductor, e.g. a diode, transistor or an integrated circuit, separated from a wafer. Also referred to as a bare die or a chip.
- DIE ATTACH Bonding of semiconductor die to a package/substrate. Same as die bonding.
- DIE ATTACH Adhesive attachment of a semiconductor die to a package/substrate. Can be thermally conductive or non-thermally conductive.
- DIE BONDING The process of attaching a semiconductor die to a package, substrate or board with a eutectic or solder alloy.
- DIE BONDER The machine used for die bonding.
- DIELECTRIC Any material that does not conduct electricity, an insulator, such as glass, ceramic or epoxy. Sometimes used to refer to a nonconducting ink or paste.
- DIELECTRIC BREAKDOWN VOLTAGE The threshold voltage that causes a dielectric layer to conduct electricity.
- DIELECTRIC CONSTANT A property of a dielectric material that is a measure of the ability of a material to store an electric charge.
- DIELECTRIC LAYER- A film of insulating material separating two conductor films or as an insulating layer on a metal surface to allow deposition of a layer

of conductive circuitry. Also refers to application of an insulator to function as a passivation layer.

- DIELECTRIC LOSS The power lost in a dielectric layer when placed in an A/C field.
- DIELECTRIC STRENGTH The maximum electric gradient a dielectric layer can withstand without breaking down. Expressed in units of volts/mil.
- DIE-SHEAR TEST A test to determine the shear strength of the bond between a die and the base it is bonded to.
- DIFFUSION The movement of atoms from regions of high concentration to low concentration. Diffusion depends on temperature, concentration and the mobility of the specific material.
- DIRECT BOND COPPER (DBC) The high temperature direct bonding of copper foil to a ceramic by means of the copper-oxygen eutectic.
- DIRECT CHIP ATTACH (DCA) Refers to the assembly of bare die to a package, substrate or board.
- DISCRETE COMPONENT Packaged active or passive devices as opposed to bare die.
- DISSIPATION FACTOR Tangent of the dielectric loss angle. The ratio of the resistive component of a capacitor to the reactance.
- DOUBLE SIDED BOARD A printed wiring board with conductive circuitry on both sides of the board.
- DRY AIR Air that has had moisture removed. Dryness is specified by the dew point, e.g. –40°C.
- DRY FILM RESIST A relatively thick (.12.5 mils) photosensitive film applied by lamination.
- DRY PRESSING A method of making ceramic parts whereby ceramic powder is compacted in a mold and fired in a furnace to sinter the powder.
- DRY PRINT A thick film print that has gone through the drying stage.
- DUAL IN LINE PACKAGE (DIP) A package having two rows of leads, with equal spacing on two opposing sides and designed for through-hole attachment onto a printed wiring board.
- DUCTILITY The ability of a material to be deformed without fracture.

Е

- EDGE DEFINITION/EDGE ACUITY The sharpness of a pattern deposited by a thick film or thin film process. See Definition.
- ELECTRICAL ISOLATION Separating two or more conductors from each other by means of a dielectric.
- ELECTROLESS DEPOSITION The deposition of an electrically conductive film from an autocatalytic plating solution without the use of electric current.
- ELECTROPLATING The deposition of an electrically conductive film from a solution (plating bath) of the ions of that metal, by means of an electric current.
- ELECTRONIC PACKAGING A process involving the interconnection of semiconductor devices into packages (single or multichip), substrates or boards to complete the manufacture of a fully functional electronic system or subsystem.
- ELEMENT A bare unpacked die typically referring to an Integrated Circuit.

272 Integrated Circuit Packaging, Assembly and Interconnections

- ELEMENT EVALUATION Assembly and electrical testing of a sample of bare die taken from a manufacturing lot to assess the electrical integrity (number of parts electrically good following assembly and burn-in) of the particular die lot. Also called a Lot Acceptance Test (LAT).
- ELONGATION The ratio of wire length at rupture to original length. A measure of ductility. Measured in percent.
- EMBEDDED LAYER A conductive or passive layer deposited between two dielectric layers.
- EMULSION In screen printing, the light sensitive material used to pattern coat a mesh screen. When exposed and patterned it is used for depositing distinct patterns of thick film paste that are subsequently dried and fired.
- ENCAPSULANT A material that seals or covers a semiconductor to provide mechanical and environmental protection. Typical materials are: molding compound, glob top, dam & fill and potting compound.
- ENCAPSULATE To coat or cover with an organic material (epoxy or silicone) an assembled device to provide mechanical and environmental protection.
- ENVIRONMENTAL TEST A test to determine the integrity of an electronic assembly under various external conditions.
- EPOXY A family of thermoset or thermoplastic polymers used in microelectronic packaging for bonding, encapsulation, and underfilling.
- EPOXY Family of thermosetting resins that are used as the media for bonding and/or protecting semiconductor devices. The main advantages of epoxy are the ability to form strong bonds to many surfaces, low processing temperature and low cost. Epoxies come in many variations with different properties.
- ETCHED METAL MASK A metal foil where the pattern is made by a wet or dry etches process.
- ETCHING The process of removing unwanted material by wet (chemical) or dry (plasma) processes using appropriate masking (a resist or another metal).
- EUTECTIC The metallurgical composition two or more metals (alloy) that has a melting point significantly lower than that of the higher melting metal.
- EUTECTIC TEMPERATURE The melting temperature of a specific eutectic alloy composition.
- EXPOSURE The process of transferring a pattern from a photomask to a photosensitive film coated wafer or substrate by using an appropriate energy source, such as ultraviolet light, laser, e-beam or x-ray.

F

- FAILURE ANALYSIS A process to determine reasons why a device, circuit or assembly does not meet performance specifications.
- FAILURE MECHANISM A process intended to determine cause for the failure of a device, circuit or assembly fails to meet its intended performance specifications, e.g., and open or shorted conductor trace.
- FAILURE RATE The ratio of the number of failures to the total number tested. Usually specified as %/1000 hours of operation.

- FATIGUE With solder bonds, a failure mechanism caused by exposure to repetitive levels of mechanical stress over time resulting from mismatch in thermal coefficient of expansion, e.g. a bare die and an organic substrate or board.
- FEEDTHROUGH A method of making electrical connection between both faces of a circuit board, substrate or package, e.g., a plated through-hole or through a package wall.
- FILLED POLYMER The addition of a powder (ceramic or metal) to change the thermal and/or electrical properties of the polymer e.g. silver particles to an epoxy to increase electrical conductivity or born nitride to an epoxy to improve thermal conductivity.
- FILLER The general term for any addition agent into a material to change its properties, i.e., electrical and/or thermal conductivity.
- FILLET Refers to the extension around the edge of a die from the adhesive or alloy used in bonding a die to a package, substrate or board.
- FILM Any thin layer on the surface of a substrate such as a thick or thin film conductor or dielectric, or a layer of moisture, or contaminant.
- FINAL SEAL The manufacturing operation wherein a lid is attached soldering, welding or with an epoxy that completes the enclosure of a microcircuit into a package with a controlled ambient.
- FIRING The process of heating screen printed thick film materials to an elevated temperature in a furnace, to transform the paste into its final functional form.
- FIRST BOND In chip and wire assembly, the first bond in a sequence of two or more bonds made to a wire.
- FLAT PACK A package for microcircuits having the leads extending from 2 opposing sides and designed specifically for surface mounting onto a printed wiring board.
- FLEX CIRCUIT Interconnect circuitry supported on a thin flexible organic film (Kapton®/polyimide), typically 25 micrometers thick. Circuitry can be single sided, double sided or multilayer.
- FLEXIBLE COATING A polymer film that remains non-rigid after curing.
- FLIP CHIP (FC) A leadless device typically an integrated circuit that is designed to be attached, face down to a package, substrate or board by means of bumps on deposited each bond pad. No wire bonding is used. The flip chip is bumped typically while in wafer format.
- FLIP CHIP ATTACHMENT The process that completes the electrical connection of an active device by facedown bonding to a package/substrate.
- FLUX In soldering, a resinous material the dissolves oxides and improves wetting of a solder to a metal surface.
- FLUX RESIDUE Soldering flux remaining after soldering and cleaning.
- FOIL A thin continuous sheet of metal, usually copper, applied to an organic board by cladding and subsequently patterned as conductor traces.
- FOLDED FLEX PACKAGING Stacked packages interconnected using flex circuitry.
- FORMING GAS A mixture of H_2 and N_2 , typically less than 5% H_2 . Used wherever a reducing non-oxidizing atmosphere is needed, e.g., eutectic die bonding or fluxless soldering.

274 Integrated Circuit Packaging, Assembly and Interconnections

- FRONT END In semiconductor manufacturing: refers to those manufacturing processes in which multiple integrated circuits are formed in and on a semiconductor wafer. Front end processes end with wafer electrical testing.
- FUNCTIONAL CIRCUIT ELEMENTS Refers to bare die, i.e., diodes, transistors and integrated circuits.

G

- GALLIUM ARSENIDE (GaAs) A semiconductor typically used for high-speed, high frequency circuit applications.
- GLASS BINDER The glass powder added to a thick film ink to hold the functional particles together and to promote adhesion to the surface of the ceramic.
- GLASSIVATION A method of passivating a semiconductor die by coating with a glass layer leaving only the bond pads exposed.
- GLAZE General term for a glass coating.
- GLAZED SUBSTRATE A ceramic substrate that has been coated with a glass layer for smoothness.
- GLOB TOP An epoxy encapsulant. Typically used for Chip on Board.
- GRAM-FORCE In wire bonding or flip chip attachment the amount of physical force required to create an open bond.
- GREEN A term used to identify an unfired ceramic sheet or tape. For example, a "green" substrate is one that has been formed, but has not been fired.
- GROUND PLANE A conductive layer used as a common reference point for one or more electrical connections.

Η

HALOGENS - The elements Chlorine, Fluorine, Bromine and Iodine.

- HALOGENATED SOLVENTS Organic liquids containing one or more of the halogens. Generally used as cleaning solvents. For example, trichloroethane.
- HARD SOLDER Solders containing Au, e.g., 80%Au/20%Sn, melting point 280°C.
- HARDNESS A material property. The ability of a material to resist penetration.
- HARDNESS Property of a material to resist indentation or scratching.
- HEAT SINK A piece of high thermal conductivity material slightly larger than the component (bare die or packaged) used to conduct heat away from the heat-sensitive device. Examples are most metals and diamond.
- HEEL OF THE BOND In wire bonding, that part of the wire where deformation begins. It is noted on the first and second bond in wedge bonding and the second bond in ball bonding.
- HEEL BREAK A break in a bonded wire at the heal of the bond.
- HERMETIC SEAL Capping of a package containing an active device to provide an enclosure that maintains a controlled ambient.
- HIGH TEMPERATURE CO-FIRED CERAMIC (HTCC) A monolithic multilayer ceramic package or substrate containing an embedded conductor interconnect circuit. Individual layers of ceramic with patterned conductor traces (typically

tungsten or molybdenum) are processed separately, inspected, collated, stacked and co-fired at temperatures in the range of 1400 to 1600°C.

HI-K CERAMIC - A ceramic material with high dielectric constant.

HIGH PURITY ALUMINA - Alumina with over 99.9% Al₂O₃ content.

- HOSTILE ENVIRONMENT An environment that has a degrading effect on an electronic device or assembly e.g. automotive or space environments.
- HYBRID CIRCUIT (HC) A multi-component assembly containing active devices (bare or packaged) and passives (deposited or discrete) interconnected on a rigid insulating substrate (ceramic or organic) by a deposited (thick or thin film) conductor network that can be single or multilayered. Also referred to as Hybrid Integrated Circuit (HIC) or Hybrid Microcircuit.

I

- INERT ATMOSPHERE A gas atmosphere composed on one of the inert gases, i.e., non-oxidizing, non-reducing. Ar or N_2 are most commonly used.
- INFANT MORTALITY Early device electrical failures occurring when subjected to stress conditions, e.g., burn-in testing. Electronic components are generally characterized by an initially high failure rate that decreases with increasing time. (Bathtub curve).
- INJECTION MOLDING Molding of electronic packages by forcing a heated liquid epoxy into a steel mold containing the parts to be encapsulated.
- INK or PASTE A general term for screenable thick film compositions.
- INSERTION LOSS The difference between power received at the load before and after the insertion of a device in the line.
- INSPECTION LOT A sample quantity of devices, representing a production lot, submitted at one time, to determine compliance with acceptance requirements as specified on the procurement documents.
- INSULATORS A class of materials with high insulation resistance. Also refers to thermal or electrical insulators.
- INTEGRATED CIRCUIT (IC) A microcircuit or microchip. A single semiconductor die (Si, GaAs, SiGe) containing multiple transistors interconnected by a single or multiple layers of patterned conductors, each separated by a layer of dielectric. This monolithic structure may also contain passive elements as well. An IC is also referred to as microcircuit or microchip.
- INTERCONNECTION Use of conductive metal, e.g. wires, bumps and packages or substrates with embedded conductor circuitry, to electrically link a single device or multiple devices with each other.
- INTERFACE The boundary between two materials, e.g. in wire bonding the area of contact between the wire and the metal bond pad or between a deposited metal and an electro or electroless plated metal.
- INTERMETALLIC COMPOUND (IMC) A compound of two or more metals that have a characteristic crystal structure and defined composition. Referred to simply as Intermetallic, an IMC is characteristically brittle and high resistivity.
- ISOTROPIC As related to etching of films, etch rate the same in all directions x, y and z. Also relates to conductive adhesives, electrically conductive in all directions x, y and z.

J

JUNCTION TEMPERATURE – The temperature in the region of transition between p- and n- type semiconductor in a transistor structure. Excessively high junction temperature can degrade device reliability and lead to complete failure.

K

- KIRKENDALL EFFECT The occurrence of void formation in a material caused by diffusion of atoms across an interface the result of exposure to elevated temperature. Excessive voiding can result in an electrical open.
- KNOWN GOOD CIRCUIT (KGC) A circuit that has been tested to preclude presence of destructive defects that after assembly of all elements and components would not be electrically functional.
- KNOWN GOOD DIE (KGD) A qualification or process that verifies an unpackaged semiconductor die has been electrically tested to a specific level of quality and/or integrity relative to the packaged device's electrical specifications.

L

- LAMINAR FLOW A constant directional flow of highly filtered air across a work surface or area. The flow can be parallel or perpendicular to the work surface.
- LAMINATE A layered structure of sheets bonded together under heat pressure.
- LAMINATE THICKNESS In a printed circuit board, the thickness of the core and metal cladding prior to further processing.
- LASER TRIM The upward adjustment of a film resistor by cutting and physically removing material by means of a laser.
- LAYOUT A dimensioned drawing of a patterned circuit containing conductor traces and deposited passives. Used in the fabrication of thick film screens or photomasks. The layout is typically at some magnification, e.g. 10X, and is subsequently photographically reduced to 1X on a master plate or film that is used to produce a screen or mask.
- LEACH In soldering: the dissolution of a metal into molten solder. Leaching can ensure proper bonding to the metal is achieved. Excessive leaching can result in a poor solder bond.
- LEAD Part of a package. Rigid or semi-rigid the leads are the external I/Os of the device and allow electrical and mechanical access and subsequent attachment of the package to the next assembly level.
- LEAD FRAME A metal frame that has been patterned by etching or stamping with defined leads and a base tab, to which a bare die is attached and wire bonded. The assembly is transfer molded except for the leads. All plastic packages DIPs, FPs, QFPs, are lead frame based.
- LEADLESS DEVICE A semiconductor carrier or package having no input/output external leads extending out from the package body.
- LEADLESS INVERTED DEVICE (LID) A ceramic package designed specifically for transistors (late 1950s) for use on hybrid circuits. It had no leads but rather

metallized pads for solder attachment directly onto a ceramic substrate. It was the first semiconductor package that to be surface mounted.

- Level 1.0 INTERCONNECTIONS Refers to the assembly of bare die to a package, substrate or board.
- Level 1.5 INTERCONNECTIONS Refers to the assembly of multiple bare die to a package or substrate (Multichip Packaging).
- LEVEL 2.0 INTERCONNECTIONS Refers to the assembly of bare die, packaged components and discretes to a printed wiring board or ceramic board a Printed Wiring Board Assembly, a PWBA, or a Printed Circuit Board a PCB.
- Level 3.0 INTERCONNECTIONS Refers to assembly of printed circuit boards to another printed wiring board called a "mother board".
- LEVELING In thick film screen printing: The settling of thick film paste after printing. Leveling can minimize screen mesh marks in the printed paste.
- LIFE TEST The test of a component or assembly typically under actual use conditions or accelerated temperature for an extended period of time.
- LINE CERTIFICATION Verification that a production process meets applicable process procedures, specifications and control standards.
- LINE DEFINITION A measure of the dimensional exactness and quality of a patterned feature, e.g. a conductor trace, as replicated from an image on a screen or photomask.
- LINES Another term for a patterned conductor trace.
- LIQUIDUS The temperature above which an alloy is completely molten. The temperature where melting is completed for a non-eutectic alloy.
- LIQUID RESIST A photosensitive liquid generally applied to a substrate by spinning. Other techniques include spraying, dipping, curtain coating meniscus coating and electrodeposition.
- LITHOGRAPHY The transfer of a pattern or image from one medium to another, e.g. from a photmask to a photosensitive film (resist) deposited onto a wafer or substrate. Resist requires exposure to an appropriate energy source ultraviolet light, electron beam, laser or x-rays. If light is used to affect the transfer, the term "photolithography" applies.
- LOOP The wire profile formed by a bonding wire between the first and second bonds.
- LOOP HEIGHT The maximum distance of the wire loop from the surface of the first bond.
- LOSS TANGENT The ratio of irrecoverable to recoverable part of electrical energy introduced into an insulating material by the establishment of an electric field within the material.
- LOW LOSS SUBSTRATE A substrate that absorbs little energy when subject to high frequencies and is therefore suitable for microwave applications.
- LOW TEMPERATURE COFIRED CERAMIC (LTCC) Multilayer ceramic circuit package similar to HTCC but fired at temperatures 850–1000°C usually with thick film gold paste instead of refractory metals such as tungsten or molybdenum.

М

- MASK A metal foil, a polyester film or a glass plate that contains well defined features or images used for the patterning of deposited films or for the manufacture of screens for screen printing of thick film pastes.
- MESH SIZE The number of openings in a screen. A 350 mesh screen has 350 openings per linear inch or 105,625 openings per square inch.
- MEAN TIME BETWEEN FAILURES (MTBF) Used to express failure rate.
- METAL MASK A foil or thin sheet of metal, a stencil into which appropriate features have been generated by selective chemical etching.
- METALIZATION The metal film on a semiconductor die used to connect electrically different areas on the die. A film pattern (single or multilayer) of conductive material deposited on a substrate to interconnect electronic components, or the metal film on the bonding area of a substrate which becomes a part of the bond and performs both an electrical and a mechanical function.

MICROCHIP/MICROCIRCUIT - An integrated circuit.

- MICROELECTRONICS The area of electronic manufacturing specifically associated with *assembly and packaging of semiconductor die*, i.e., diodes, transistors and integrated circuits, covering single chip packaging, multichip packaging and chip on board applications.
- MICROCRACK A small crack, usually not visible to the naked eye.
- MICROSTRIP A microwave transmission component.
- MIGRATION An undesirable phenomenon whereby metal ions, e.g., silver, are transmitted across an insulated surface, in the presence of adsorbed moisture and an electrical potential.
- MIL SPEC A Military Specification.
- MODULUS OF ELASTICITY Modulus is the amount of force per cross-sectional area of a material (stress) required to change the shape of the material divided by the amount of change in shape (strain). For example, it is the force applied to a steel rod that is required to cause the rod to stretch or get longer divided by the amount the rod stretches. Modulus is a measure of the flexibility or elasticity of a material. The lower the number the more elastic the material. A rubber band has a very low modulus because it stretches very easily. An aluminum bar has a higher modulus because it takes more force to stretch it. Glass has a very high modulus; it will usually break before it stretches.
- MOISTURE STABILITY The stability of a component or material under the conditions of high humidity.
- MONOLITHIC INTEGRATED CIRCUIT An integrated circuit.
- MOS DEVICE Abbreviation for Metal Oxide Semiconductor device.
- MOTHER BOARD A circuit board used to interconnect smaller circuit board assemblies.
- MULTICHIP MODULE (MCM) A multichip assembly similar to a hybrid circuit, but of a higher level of complexity comprised of at least two Very Large Scale Integration ICs. The MCM is designed and structured to be supportive of the electrical, mechanical and thermal needs of the ICs.

- MULTICHIP PACKAGING (MCP) A packaging option in which multiple chips are assembled into a package. MCP generically covers Hybrid Circuits, Multichip Modules, and System in Package, System on Package and Stacked Die.
- METALLIZATION Refers to metal interconnections on a wafer, package, substrate or board.
- MULTILEVEL METALLIZATION Two or more levels of metal (circuitry) forming electrical interconnections for active and passive components, discrete or deposited, to create a functioning electronic circuit. Individual metal layers are isolated from each other by a dielectric. Vias in the dielectric allow for interconnection between the metal layers.

Ν

NECK BREAK – In ball bonding, a wire breaks directly above the ball bonds.

NEGATIVE IMAGE – The reverse image of the to-be-patterned feature.

NONCONDUCTIVE EPOXY – An epoxy material (a polymer resin) of very high electrical resistivity.

- OFF CONTACT (1) In screen printing, the normal printing set up whereby the screen is not in contact with the substrate prior to the printing stroke. (2) In Thin Film Photolithography, a printing mode where mask is not in direct contact with photosensitive resist on the wafer, substrate or board. Also called Proximity Printing.
- OHMIC CONTACT An electric contact that has a linear voltage vs. current relationship. It is a measure of the electrical conductivity of a bond and is expressed in terms of milliohms.
- OHMS PER SQUARE A measure of the electrical resistivity or sheet resistance of a conductor film.
- ORGANIC FLUX A solder flux composed of rosins and organic solvents.
- OUTGAS Relates to the amount of weight loss of an adhesive during curing or at elevated temperatures due to solvent evaporation. Any solvent or low boiling temperature components of a polymer formulation can evaporate. The temperature and conditions entirely depend on the materials of the formulation. Bubbles, formed as the outgas materials tries to escape, can form voids in the die attach, underfill or encapsulant. These vapors can also condense on nearby die bond pads and package pads and interfere with wire bonding.
- OVERCOAT A thin coating of insulating material applied to a component or assembly for the purpose of providing additional mechanical and environmental protection (may be organic or inorganic).
- OVERGLAZE An inorganic coating of a fired thick film paste composed of glass frit.
- OXIDIZING ATMOSPHERE Gaseous ambient containing oxygen.

- Р
- PACKAGE An enclosure or carrier, metal or plastic, for a semiconductor die or substrate assembly, with I/O terminals to provide electrical access and attachment to the next assembly level. Both metal and plastic packages provide for mechanical protection from damage. The metal package however affords the highest level of environmental protection by providing a hermetic enclosure, i.e. a controlled and constant ambient, for the device(s).
- PACKAGE LID A flat metal plate used to completely seal a package cavity to provide a hermetic enclosure.
- PACKAGE on PACKAGE (PoP) Stacked packages.
- PAD That portion of a conductive pattern designed for device attachment. e.g., die bonding, wire bonding.
- PANEL A large substrate. Typically refers to the organic substrate used in printed wiring board manufacturing.
- PASSIVATION An insulating layer (organic or inorganic) deposited directly over a circuit element to protect the surface primarily from ionic contaminants, moisture and mechanical damage. See OVERCOAT.
- PASSIVE COMPONENTS Components that do not change their basic character when an electrical signal is applied, e.g., resistors, capacitors and inductors.
- PASSIVE NETWORK A circuit composed of multiple passive devices, deposited or discrete.
- PEEL STRENGTH In thin films, it is the force required to peel or strip a deposited film from a substrate. It is typically expressed as a gram-force.
- PELLICILE An optically transparent membrane mounted on a machined metal frame and attached to a reticle to prevent airborne contaminants or damage from handling. Contaminants on the membrane surface are out-of-focus during exposure.
- PHASE DIAGRAM Also known as an equilibrium diagram. A chart, generally, of two or more elements (an alloy) showing their phases over temperature and composition range when equilibrium has been reached.
- PHOTOETCH A process of patterning a metal film by exposing and developing a photosensitive film and using the resist as a mask to etch away exposed metal.
- PHOTOETCHABLE THICK FILM A post-fired thick film patterned using photoresist as an etch mask.
- PHOTOIMAGABLE THICK FILM A fully screened, pre-fired, thick film that is inherently sensitive to ultra violet light and can be patterned without using a photoresist and does not require chemical etching.
- PHOTOMASK Glass plate containing a pattern or image (positive or negative) to be transferred to a wafer or substrate. Used in the photolithographic process, each pattern consists of opaque areas that prevent ultra violet light from passing through and exposing an underlying photosensitive resist. Following a development step patterning of the resist is complete and can be used as a mask for etching or as a plating template.
- PINHOLE Small voids that occur in a deposited film.
- PITCH The sum of the width of a trace and the space separating two adjacent traces.

- PLANARIZATION The deposition of a film such that the surface of the film is relatively flat and unaffected by the underlying topography. Planarization is strongly dependent upon the material properties (e.g., solids content and the thickness of the coating). A planar coating is the opposite of a conformal coating.
- PLASTIC ENCAPSULATED MICROCIRCUIT (PEM) A device encapsulated with an organic material.
- PLASTIC ENCAPSULATION Mechanical and environmental protection of a completed device by embedding it in a plastic, typically an epoxy.
- PLASMA An ionized gas composed of equal number of positive and negative charges.
- PLATED THROUGH-HOLE (PTH) A hole in an organic substrate made conductive by plating the non-conductive sides of the hole to allow electrical connection from one surface to the other. The electrically conductive PTH also makes connection to inner conductor layers in a multilayer printed wiring board.
- PLUG IN PACKAGE A package with leads arranged such that they can be inserted into a socket in the vertical direction as opposed to the longitudinal direction, e.g. a flatpack.
- POLYIMIDE An insulating polymer derived by condensing an anhydride and diamine. With high Tg it used as the base material for printed wiring boards requiring higher temperature processing. Used also as an interlayer dielectric in thin film multilayer interconnects.
- POLYMER Compounds consisting of large molecules made up by a linked series of short molecules called monomers. When the shot molecules join together to form the long molecules, the material is said to have cured or polymerized. The structure of the polymer contributes most of the physical characteristics of the materials containing them.
- POLYMERIZE Bonding of two or more monomers to form a polymer. The process of polymerizing is also called curing.
- POROSIT A measure of the quality of a film, conductive or insulating, with respect to the absence of voids.
- POSITIVE IMAGE The true picture of a pattern, as opposed to the negative.
- POTTING COMPOUND Resin used to encapsulate or seal large areas of a device or combination of devices. Potting compounds are normally poured or dispensed into a device enclosure, filling the entire area.
- PREFORM A sheet of material, punched into a specific shape. Preforms are typically used for die or substrate attach, e.g., solder preforms or epoxy preforms.
- PREPREG Sheet material (e.g., glass fabric) impregnated with a resin cured to an intermediate stage (B-stage resin).
- PRE SEAL VISUAL The process in which a device or assembly is visually inspected prior to final lid sealing.
- PRESSED ALUMINA A method of making alumina parts, such as substrates, by pressing the powder in a mold and then firing.
- PRINT & FIRE A term associated with the thick film patterning process. It specifically refers to post-screen printing processing of a thick film paste that completes the patterning process.

- PRINTED CIRCUIT BOARD (PCB) A printed wiring board with assembled components. Also referred to as a Printed Wiring Board Assembly (PWBA).
- PRINTED WIRING BOARD (PWB) A organic based substrate/board single, double-sided or multilayer with photopatterned conductor traces on both sides and all inner layers in multilayer structures forming an electrical interconnect circuit structure.
- PRINTING PARAMETERS Operating conditions that affect the screening operation such as off-contact spacing, squeegee speed, squeegee pressure, etc.
- PRODUCTION LOT Parts manufactured on the same production line(s) by means of the same production techniques, materials, controls, and design at the same time. The production lot is usually date coded to permit control and traceability as required for maintenance of reliability programs.
- PROJECTION PRINTER A photolithography exposure system that exposes an image onto a wafer or substrate by optically projecting the image from the mask. There is no physical contact between the mask and the wafer or substrate. The mask used on a projection printer is referred to as a reticle.
- PULL STRENGTH In wire bonding, it is a measure of the strength of a fully bonded wire when subjected to a destructive force, as in wire pull testing.
- PURPLE PLAGUE One of several gold-aluminum intermetallic compounds (IMC) formed when bonding gold to aluminum and activated by exposure to elevated temperature. The IMC is purple in color and very brittle that eventually leads to failure of the bond.
- PULL TEST A test to measure the amount of force needed to destructively cause a bonded wire to fail.
- PUSH OFF STRENGTH In wire bonding, the amount of force (in pounds or grams) required to separate a wedge bonded wire or a ball bond from a metal-lized bond pad.
- PUSH OFF TEST A test to determine quality of a bonded wire or a deposited bump.

Q

QUARTZ – Single crystal SiO₂.

R

REACTIVE or REFRACTORY METALS – A class of metals or alloys that have similar characteristics including very low electrical conductivity and very high melting temperatures. Used as conductor material in high temperature cofired ceramic (HTCC) processing requiring firing temperatures in excess of 1200°C. Readily oxidizing, a reducing atmosphere is necessary during firing. Refractory metals include molybdenum (Mo), and tungsten (W).

REAL ESTATE – Refers to the total surface area of a chip, substrate or board.

REDUCING ATMOSPHERE – An atmosphere in a furnace or oven, typically containing hydrogen, and used to prevent oxidation of parts.

- REFLOW SOLDERING Soldering technique involving application of solder followed by heating in a furnace or oven to a temperature above the melting point of the solder. The parts are bonded upon cooling and solidification of the solder.
- REGISTRATION The proper positioning of a substrate or board; the alignment of a screen or photmask to another circuit pattern on a substrate or board.
- REGISTRATION MARKS Marks used for positioning and used for aligning of photomasks for multiplayer structures.
- RESIN An organic substance that is polymeric in structure and predominantly amorphous.
- RESIST Same as Photoresist. A photosensitive coating when exposed and developed provides a patterned template for etching or selective plating.
- RETICLE A photomask used on projection printers. Typically contains a single image at IX or 5X, 10X or a grouping of the same image also at magnification.
- REWORK All work performed, except testing, on a circuit after initial fabrication in order to replace defective parts for compliance with specifications.
- RHEOLOGY Refers to the flow properties of liquids.
- ROSIN FLUX An organic acid used to clean mating surfaces prior to or during soldering.

S

SAPPHIRE – Single crystal aluminum oxide.

- SCANNING ELECTRON MICROSCOPE (SEM) A microscope that uses a beam of electrons for viewing small objects at very large magnification.
- SCHEMATIC A representative drawing in a symbolic format of an item, e.g. a process flow chart, or a detailed diagram of a functional electronic circuit.
- SCREEN A network of interwoven metal wire or fabric (a mesh) mounted on a solid frame. Upon application and selective patterning of an emulsion film on one side of the mesh the screen is ready for thick film printing.
- SCREEN FRAME A metal or plastic frame that holds the screen taut and serves as a means of mounting the screen onto the printer.
- SCREEN PRINTING The process of transferring an image to a substrate by forcing a paste, using a squeegee, through a selectively masked stencil screen.
- SCRIBE LINE The lines that separate the die from each other on a wafer. It is also referred to as the "street". It is where the dicing or singulation occurs.
- SCRUBBING Agitation of a silicon die on a gold bonding pad, at elevated temperature, to form a eutectic.
- SECOND BOND In wire bonding, the last bond that completes the attachment of the wire.
- SELECTIVE PLATING An electroplating technique whereby only certain areas are plated, typically using a patterned photoresist as the mask.
- SEMICONDUCTOR A materials that has an electrical conductivity between a conductor and an insulator. The conductivity can be changed by the introduction of impurities and the creation of selected areas with different carriers of current, i.e. electrons (n-type) and holes (p-type) and the formation of a p-n junction that is the building block of a solid-state diode, transistor, and integrated circuit.

284 Integrated Circuit Packaging, Assembly and Interconnections

- SHEET RESISTANCE The electrical resistance of a thin sheet of material with uniform thickness as measured across opposite sides of a unit square and is expressed in ohms/square.
- SHELF LIFE The useful life of a material, after date of manufacture. Shelf life may vary from minutes, in the case of mixed epoxies, to years.
- SILICON THRU VIA A chemically etched through hole in a silicon die, filled or plated to provide electrical connectivity. Used as the vertical interconnect for stacked die. Requires specially designed ICs.
- SINGLE SIDED BOARD A PWB with circuitry on one side only.
- SIINGULATION The process of separating individual die from a wafer.
- SINTERING The heating at an elevated temperature of two or more metals to allow interdiffusion to occur to enhance the bonding between the materials involved.
- SKIN EFFECT The increase in resistance of a conductor at microwave frequencies due to the tendency of current to concentrate at the conductor surfaces.
- SLUMP The tendency of a thick film ink to spread after printing causing vertical walls of a conductor to spread out diagonally.
- SOFT SOLDER A low temperature (generally below 300°C) melting solder alloy, e.g. eutectic SnPb 63/37.
- SOLDERABILITY The ability of a metal to be wet by solder.
- SOLDER BALLS Large solder bumps typically >200 micrometers in diameter. Solder balls are used for attachment of area array packages, e.g. BGAs, CSPs.
- SOLDER BUMPS Small balls of solder <200 micrometers in diameter used to make electrical connections on face down bonded flip chips and Wafer Level CSPs.
- SOLDER DAM A solder mask. A non-solderable material applied across a conductor to limit the spreading of molten solder. Applied by screening or dry film lamination.
- SOLDERING The process of joining parts, typically metals, by melting and solidification of a metal or metals (an alloy) having a melting point that is below that of the parts being bonded.
- SOLDER RESIST A solder mask. A photosensitive organic material patterned for selectively depositing solder material.
- SOLVENT RESISTANT The degree to which a material is unaffected by solvents.
- SPUTTERING The process of removing atoms from a source target by means of a high voltage created plasma. The dislodged atoms are deposited as a thin film onto a substrate.
- SQUEEGEE The part of a screen printer used to physically force thick film paste through a screen.
- STEATITE A ceramic composed of magnesium, aluminum and silicate.
- STENCIL A metal foil with patterns selectively etched through the foil. Stencils as opposed to screens are used where thicker films are required, e.g. solder paste is stencil printed rather than screen printed.
- STEP AND REPEAT PROJECTION PRINTER An exposure system in which the wafer or substrate onto which an image is projected is indexed from site to site in order to completely expose an entire wafer or substrate. Referred to as a Stepper.

- STITCH BOND The second bond in ball bonding.
- STRESS FREE A material state in which there is little or no internal forces causing stress.
- STRESS RELIEF- The process of making a material stress free. Usually by heating (annealing).
- STRIPLINE A planar microwave transmission geometry consisting of a center conductor surrounded on both sides by an insulator.
- SUBSTRATE The base material upon which passivation layers, metallizations and circuit elements may be added to build a device, package or an assembly.
- SURFACE FINISH For substrates: A measure of the smoothness of the surface. For PWBs: The overplating of copper traces to accommodate various component attachments, e.g., soldering, wire bonding.
- SURFACE MOUNT Component attachment wherein all connections, typically solder, are made on the top surface circuitry rather than into sockets or plated through holes.
- SURFACE TENSION- A force that exists between liquids and a surface.
- SURFACTANT A contraction of the words surface active agent. A chemical that promotes wetting with a liquid.
- SYSTEM IN PACKAGE (SiP) A packaged component providing full system functionality. It can refer specifically to a single package containing stacked die with all die are the same device technology, e.g. CMOS. Wire bonding is the dominant means of interconnecting the stacked die.
- SYSTEM ON PACKAGE (SoP) Same as SiP or more specifically a packaged component with full system functionality like an MCM but with stacked die, single and stacked packages. It accommodates different device technologies, Si, GaAs, SiGe, as bare or packaged die, as well as different die functions logic, memory, rf, analog and digital. Other technologies, MEMS as well as optical components can also be included. Passives and other components including, antennas, filters, resonators, can be added to the package. A SoP might be considered as an HDI PWB assembly reduced to a single package component in a CSP package format.

NOTE: The deference between SiP and SoP are not universally accepted within the microelectronics community. Many consider no difference and use only SiP to refer to all approaches offering full system functionality.

Т

TAPE – (1) A dried and cast homogeneous slurry of ceramic powder, sintering aids and organic binders. The cast product is formed into shape and fired to form substrates and packages. Prior to the firing the tape is often referred to as "green ceramic. (2) A term used in referring to very thin (typically 25µm thick) fully cured organic materials (e.g., Kapton®, polyimide).

- TAPE CASTING The process of casting ceramic into long, flexible sheets. Tape casting is used in the manufacturing of alumina substrates.
- TARNISH Chemical changes that occur on the surface of metals due to the action of oxygen or sulfur.
- TEMPERATURE AGING Subjecting a circuit to an elevated temperature for an extended period of time intended to reduce stress and stabilize the unit.
- TEMPERATURE CYCLING A test that subjects a device or assembly to alternating high and low temperatures over an extended period of time.
- TEST PATTERN A circuit designed to provide early evaluate electrical performance and/or properties of a device or material. For example test patterns are used on wafers as part of the in-process controls to monitor the manufacturing processes.
- THERMAL CONDUCTIVITY The rate at which heat is transferred by a material.
- THERMAL GRADIENT The changes in temperature across an interface or through a material.
- THERMAL MISMATCH The differences in thermal expansion coefficient (TCE) of materials that are joined together. A mismatch in TCE between materials generates stress when subjected to any thermo-mechanical forces. Stress can result in degradation in a joint including complete separation.
- THERMOPLASTIC An organic material that can be cured reheated and remelted without change in properties.
- THERMAL SHOCK A condition whereby devices are subjected alternately to extreme heat and extreme cold. Similar to temperature cycling but the time between to the two temperature extremes is significantly shorter and sometimes executed using a liquid-to-liquid bath.
- THERMOCOMPRESSION BONDING In wire bonding: The metallurgical attachment of a wire to a device or package bond pad by application of both temperature and force.
- THICK FILM Refers to a process and materials: A patterning process involving screen printing of a thick film paste followed by drying of the printed paste and a high temperature firing (800°C) to complete the process. Pastes are available as conductor, resistor or dielectric materials (generally greater than 10 microns thick).

THICK FILM CIRCUIT - A circuit manufactures by the thick film process.

- THICK FILM TECHNOLOGY Encompasses the thick film materials and the patterning processes.
- THIN FILM A patterning process that basically emulates the IC wafer photolithographic process. Materials are deposited, conductors typically by sputtering or electroless plating and insulators, applied by spinning and subsequently curing, or lamination. The patterning involves use of a photoresist that when patterned serves as an etch mask or a selective plate-up template. The thin film process offers the finest line resolution and highest wiring density.
- THIXOTROPIC A property of thick film pastes becoming more fluid (a decrease in viscosity) as a force is applied physically forcing the paste through the a patterned screen.
- TINNED Generally has come to mean the part has been coated with solder.

- TRANSFER MOLDING A method of packaging an IC. In a molding press a molten plastic, an epoxy, is transferred under heat and pressure into a cavity holding fully assembled devices on a lead frame.
- TRIMMING A method of accurately adjusting the value of a deposited resistor or capacitor to a desired value.

U

- ULTRASONIC BONDING In wire bonding: A wire bonding process that uses ultrasonic energy to join two metals.
- UNDER BUMP METALLIZATION (UBM) A layered metal structure deposited and patterned over Al bond pads to provide a solderable surface for the deposition or placement of solder bumps or balls for flip chip and Wafer Level CSPs.
- UNDERFILL When a die is flip chip attached the CTE mismatch of the substrate and die can create stress on the joints causing them to fail over time or extended thermal cycling. In order to reduce the stress, a polymer material is flowed or otherwise placed under the die. This material is called underfill. Underfill that flows under the die after is attached is called conventional underfill. Underfill that is placed under the die before the die is attached is called no-flow underfill.
- UNDERGLAZE A glass coating applied to a substrate to improve the surface finish prior to the deposition of any metallization.
- UV CURING The polymerization or cross linking of low molecular weight materials using ultraviolet (UV) light as the energy source.

V

- VAPOR DEPOSITION The deposition of films onto a substrate by evaporation techniques.
- VEHICLE Refers to the organic liquids (solvents or thinners) that are part of the overall make-up of a thick film paste. These liquids help in the mixing of the solid particles in the paste and at the same time help in adjusting the viscosity to improve the thick film screen printing process.
- VERTICAL INTEGRATION Die stacking where silicon thru vias provide interconnections between die.
- VIA An opening formed in a dielectric layer or substrate and metallized to create an electrical connection between two or more conductor layers.
- VISCOSITY The speed of fluid flow and/or the resistance to shear. Usually measured in Centipoise (csp).
- VITREOUS Glass like or glassy. The opposite of crystalline.
- VITREOUS BINDER A glass phase used in cermet pastes to promote adhesion.
- VOID A hole in an encapsulant, die attach adhesive or underfill is called a void. Voids can exist because air is trapped during the dispense and bond process (the hole is "surrounded" by polymer and gets trapped) or can form because the polymer releases gas during curing. Voids reduce the adhesion strength. They can also trap moisture and reduce the device reliability.

288 Integrated Circuit Packaging, Assembly and Interconnections

VOLATILES – Any material that evaporates or boils rapidly at the temperature at which it is used or processed is said to be volatile. Many organic materials that are used as solvents are volatile. If a polymer requires the use of such solvents (because it won't flow without help) it is said to contain volatile material. When volatile materials escape they can create voids and must be processed accordingly.

W

- WAFER A thin slice of semiconductor crystal. Serves as the substrate during the fabrication of the integrated circuit.
- WAFER LEVEL PACKAGE (WLP) A process (thin film) where an area array package is formed while the device is still in wafer format. Like a flip chip the package is actual die size and is therefore a CSP (a WL-CSP).

WARPAGE – See BOW.

- WAVE SOLDERING A process for soldering where board assemblies are brought into contact with a gently overflowing wave of molten solder.
- WEDGE BOND A wire bond made with a wedge tool.
- WETTING The spreading of molten solder (or glass) on a clean metal.
- WIRE BONDING A process that uses a thin wire (Au, Al, Cu) for electrically connecting a device to a package, substrate or board. Two bonds are required to complete the connection. Bonding methods include Thermocompression (requires application of heat and pressure to the wire; Ultrasonics (require application of pressure and ultrasonic energy but at room temperature), and Thermosonics (requires application of heat, pressure and ultrasonic energy). The bonding tool used determines types of bonds. A capillary produces a ball bond and a wedge tool a wedge or stitch bond.
- WIRE SAG The failure of bonding wire to maintain the loop described by the arc of the bonding tool.
- WIRE SWEEP The movement of bonding wire during the injection molding of the package. May result in shorting of adjacent wires.
- WOVEN SCREEN Refers to a particular type of screen used in thick film printing.

Z

Z-AXIS – The vertical out of plan direction.

Z-AXIS ADHESIVE – See anisotropic conductive adhesive.

Index

А

Adhesive flip chip attachment 184–188 adhesive attach summary/concerns 188 adhesive bumps 188-189 anisotropic adhesive attach 186-187 isotropic conductive adhesive attach 185-186 non-conductive adhesive attach 187-188 reliability screening tests 184 types of adhesives 185 Alternative flip chip bonding methods 183 Alternative thin film processes, multichip packaging applications 212–218 bumpless build up layer interconnect package 215 GE high density interconnect process 212 - 214low cost "chips first" multichip module 214-215 Aluminum 106-108 material properties of 107 Aluminum wire 106 Area array packages 36–42 ceramic ball grid array 38 plastic ball grid array 38-42 tape ball grid array 40 structures 40-41

B

Ball bonding process 110-112 Ball grid array 36-41 attributes 42 concerns 42-43 surface mount assembly 41–42 Bare die problem 83–86 Benzocyclobutane 204-205 Bonder development, impact of integrated circuit on 105 Bonder equipment development 103–105 Bonding/adhesive 107 Bonding development, impact of integrated circuit on 105 Bonding methods 108–110 Bonding wire 106-108 Build up technology 251 Bump deposition processes 150–160

bumping by evaporation 152–154 copper plated bumps 154–156 direct bump/ball placement 150–151 electroless Ni/immersion Au process 160 electroplated bumps 154–156 gold plated bumps 154–156 IBM C-4NP bumping process 157–159 jet printing, solder bumping by 159 stencil printing, bumping by 156–157

С

Ceramic ball grid array 38 Chip and wire assembly 103-127 adhesive bonding 107 aluminum 106-108 material properties of 107 aluminum wire 106 ball bonding process 110-112 bonder development, impact of integrated circuit on 105 bonder equipment development 103-105 bonding, bonder development, impact of integrated circuit on 105 bonding methods 108-110 bonding wire 106-108 contamination, sources of 114 copper 106-110 material properties of 107 copper wire 106-108 die/wire bonding 103-105 eutectic vs. adhesive bonding 107 handling 118 integrated circuit, end product response 120 - 125fine pitch 122-124 metallurgical compatibility, wire bonding materials 115 metallurgical concerns, surface finishes 114-117 plated deposits 117 surface conditions 115 thick film deposits 115-116 thin film deposits 117 obstacles to quality 112-114 organic substrates, wire bonding on 125-127

insuring wire bondable organic substrates 126 "soft" substrates 126-127 plastic ball grid array, wire bonding on 125-127 printed wiring board, wire bonding on 125-127 reliable wire bonding 112-114 storage 118 thermocompression bonding, advantages/ disadvantages of 109 thermosonic bonding, advantages/ disadvantages of 110 types of bonds 110 ultrasonic bonding, advantages/ disadvantages of 109 verifying wire bonding quality 118-120 wedge bonding 111 Chip on board 93-101 direct chip attach 93-101 encapsulants for chip on board 97 flip chip on board 98-100 assembly 98-100 interconnection of board 100 mountability on board 100 mounting area on board 100 process 94-98 encapsulation 96 level 2.0 assembly compatibility 96-98 quality assurance of device 100 reliability after board mounting 100 terminal design of device 100 vs. flip chip in package/wafer level packaging 100 Chip scale package 47-58 manufacturing technologies 48-52 chip scale package 49-50 embedded chip chip scale package 51-52 singulated die chip scale package 48-49 varying structures 50-51 wire bonding 49–50 micro ball grid array 52-55 reliability concerns 57-58 wafer level packaging 55-57 processes 55-57 Cleanroom classifications 18 Cofired ceramic 233–244 advanced large scale integration processes 241-243

advantages/disadvantages 241 co-fired ceramic technology 236-237 cofired ceramic tape process 237 comparing thick film, high temperature cofired ceramic, large scale integration 239-240 high temperature cofired ceramic high temperature cofired ceramic 237-238 IBM's multilayer interconnect packaging program 234-236 low temperature co-fired ceramic large scale integration 238-239 materials 240 properties 240 technology 233-244 Comparing flip chip solder bumping processes 160-161 Contamination, sources of 114 Conventional multilayer board processing 247-248 Copper 106-108 material properties of 107 resistivity 203 Copper wire 106-108

D

Die stack flip chip/wire bonded 70 Die stacking 68–71 Die using silicon thru-vias 75–77 Die/wire bonding 103–105 Direct chip attach 93–101 Dry film photoresist properties 197 Dynamic random access memory 2

Е

Electrodeposited photoresist properties 199 Electronic manufacturing 1-14 Dynamic Random Access Memory 2 integrated circuit 1-3 overview 8 physical characteristics 8-10 microelectronics 1-14 Moore's law 1-3 semiconductors 10-14 input/output impact on package 13-14 input/output count, impact at chip level 12-13 single chip pin count 11 technology drivers 3–7 levels of interconnect/packaging 4-7 manufacturing process 3-4

packaging options 4 transistor 1-14 Embedded chip chip scale package 51-52 Embedded passives 257-259 embedded discrete capacitors 258 resistor, capacitor embedding by lamination 259 technologies 258 Encapsulants for chip on board 97 End product response, integrated circuit 120 - 125Environment, manufacturing 17-19 operator protocols 18–19 Epoxies, thin film technology 204 Eutectic vs. adhesive bonding 107 Evolution, integrated circuit packaging 32-33 Exposure systems 25-27, 196, 199, 201, 206, 230, 284 printing/imaging 25-28 contact, proximity printer 26-27 projection printer 27 step/scan projection systems 27-28 wafer stepper 27-28 thin film technology 193–195

F

FED STD 209E cleanroom standards 18 Fine pitch, end product response, integrated circuit 120-125 Flat pack 34-35 Flex circuit 71–74 Flip chip xxiv, xxvii, 5, 7, 12–13, 15, 38-40, 43-45, 47-48, 55-56, 58-59, 69-70, 77-78, 98-101, 120, 129, 143-151, 153-155, 159-161, 163-167, 169-185, 187-191, 210-213, 234-235, 253-254, 261, 267-268, 273-274, 287-288 bonding processes 170 bumping processes 143-165 bump deposition processes 150-160 bumping by evaporation 152-154 copper plated bumps 154-156 direct bump/ball placement 150-151 electroless Ni/immersion Au process 160 electroplated bumps 154-156 gold plated bumps 154–156 IBM C-4NP bumping process 157 - 159jet printing, solder bumping by 159

stencil printing, bumping by 156-157 comparing flip chip solder bumping processes 160-161 comparing wafer bumping processes 161 IBM C-4 process 152-154 IBM's flip chip transistor 143–146 flip chip process 143–144 transistors to integrated circuits 144-146 polymer/bumps 161-163 conductive epoxy bumps 161-162 elastomeric bumps 162-163 solder bump materials, reflow temperatures for 147 stud/ball bumping 163-165 trends 165 wafer bumping 147-150 under bump metallization 148 bump metallurgy, selection 148-150 chemical deposition, electroless Ni/immersion Au process 149 - 150deposition by evaporation, sputtering 149 Flip chip assembly 169–189 adhesive flip chip attachment 184-188 adhesive attach summary/concerns 188 adhesive bumps 188-189 anisotropic adhesive attach 186-189 isotropic conductive adhesive attach 185-186 non-conductive adhesive attach 187-188 reliability screening tests 184 types of adhesives 185 advantages 189 alternative flip chip bonding methods 183 basic assembly 169-189 flip chip bonding processes 170 flip chip solder joint reliability 173–182 under bump metallization consumption 181 corrosion 181-182 electromigration 181 flip chip encapsulation/underfill 177 - 178intermetallic compounds 181 materials properties, organic substrates 176

silicon cratering 174, 182 solder fatigue 174–180 underfill processes 178–180 lead-free solders 182–183 reliability 182–183 solder reflow attach 183 solder reflow process 171–173 Flip chip in package/wafer level packaging, *vs.* chip on board 100 Flip chip on board 98–100 assembly 98–100 Fluoropolymers, thin film technology 204 Future 43

G

Gold, resistivity 203

Н

High density interconnect substrate interconnect 200–201 High density interconnect substrate manufacturing technologies 193–244 cofired ceramic 233–244 thick film technology 221–232 thin film technology 193–219 High density package/substrate manufacturing technologies 193–219 High temperature cofired ceramic high temperature cofired ceramic carries 237–238 Hybrid circuit 62–64

I

IBM's flip chip transistor 143–146 flip chip process 143–144 transistors to integrated circuits 144-146 Impact of integrated circuit on packaging, interconnect technology 249-251 Industry responsiveness 92 Inner lead attachment processes, tape automated bonding 135 Inorganic materials, thermal properties 208 Input/output count 32-33 Insuring wire bondable organic substrates 126 Integrated circuit 63-64 end product response 120-125 fine pitch 122-124 Integrated circuit package 31-44 Integrated circuit packaging 31-36

Interconnections 28-29

K

Known good die 81–92 addressing bare die problem 86 bare die problem 83–86 industry responsiveness 92 known good die 86–90 multichip packaging assembly 83 semiconductor assembly/packaging/test process 81–83 wafer level burn-in, test 90–91 wafer lot acceptance testing 86

L

Laminate materials 247 electrical properties 247 thermal properties of 247 Lead-free manufacturing 43–44 processing 44 Lead-free solders 182–183 Liquid crystal polymers 204 Liquid resist, properties of spin on 197 Low temperature co-fired ceramic large scale integration 238–239

M

Manufacturing technologies 15-29, 48-52 chip scale package 49-50 cleanroom classifications 20 embedded chip chip scale package 51-52 environment, manufacturing 17-19 operator protocols 18-19 interconnections 28 negative resist, comparison 25 photolithographic process 20-28 basic pattern transfer process 21 exposure systems, printing/imaging 25 - 28photolithographic tooling 21-22 photomask/reticle 21-22 photoresists 23-24 photosensitive materials 23-24 types of photomasks 22–23 positive resist, comparison 25 processes of manufacturing, overview 15 - 17silicon wafer 16 singulated die chip scale package 48-49 varying structures 50 wire bonding 49-50 Mask aligner vs. 1X stepper 200

Index

Metallurgical compatibility, wire bonding materials 115 Metallurgical concerns, surface finishes 114-117 surface conditions 115 thick film deposits 115-116 thin film deposits 117 Micro ball grid array 52-55 Microelectronics 1-14 Minimod, tape automated bonding 129 - 140Moore's law 1-3 Multichip module 65 Multichip module-C/high density interconnect 227-229 Multichip packaging 61–79 benefits 79 die stack flip chip/wire bonded 70 die stacking 68-71 die stacking using silicon thru-vias 75-77 flex circuit 71–73 hybrid circuit 61-64 integrated circuit 61-64 multichip module 65-66 neo-stack technology 74 stacked packages 68 substrate/package technologies 62 system in package/system on package 77-79 system on package vs. system on chip 78 three-dimensional packaging 71-74 three-dimensional plus technology 73 types of multichip modules 65-66 vertical interconnect processes 75-77 Multichip packaging assembly 83, 84

N

Negative resist, comparison 25 Neo-stack technology 74

0

Obstacles to quality 112–114 Operator protocols 18–19 Organic packages, interconnect substrate 245–260 conventional multilayer board processing 247–248 current status microvia high density interconnect printed wiring boards 256 embedded passives 257–259 embedded discrete capacitors 258

resistor, capacitor embedding by lamination 259 technologies 258 impact of integrated circuit on packaging, interconnect technology 249-251 build up technology 251 printed wiring board challenge 250 - 251laminate materials electrical properties 247 thermal properties of 247 level 2.0 printed wiring board 245-259 plastic ball grid array, multichip module-L 248-249 sequential laminar circuitry 253-256 IBM 253-256 level 2.0 high density interconnect printed wiring board 255-256 technology status 259 vias, high density interconnect 251-253 microvias 252-253 Organic substrates, wire bonding on 125 - 127insuring wire bondable organic substrates 126 "soft" substrates 126-127

P

Packaging options, chip on board 93-101 chip on board 93-101 vs. flip chip in package/wafer level packaging 100 chip on board process 94-98 encapsulation 96 level 2.0 assembly compatibility 96-98 direct chip attach 93-101 encapsulants for chip on board 97 flip chip on board 98–100 assembly 98-100 interconnection of board 100 mountability on board 100 mounting area on board 100 quality assurance of device 100 reliability after board mounting 100 terminal design of device 100 Pattern transfer process 20, 21 Patterning process, thin film technology 195 - 200Photolithographic process 20–28 basic pattern transfer process 21 exposure systems, printing/imaging 25 - 28

contact, proximity printer 26-27 projection printer 27 step/scan projection systems 27-28 wafer stepper 27-28 photolithographic tooling 21-22 photomask/reticle 21-22 photoresists 23-24 types of 24-25 photosensitive materials 23-24 types of photomasks 22-23 Photolithographic tooling, photomask/reticle 21 Photomask, thin film technology 196 Photomask/reticle 21 Photoresist, thin film technology 196–199 Photoresists 23 types of 24-25 Photosensitive materials 23 Photosensitive/photodefinable thick film patterning 230-232 Physical characteristics of integrated circuit 8 - 10Pin grid array 36–41, 263 ball grid array 36-41, 262 Plastic ball grid array 38-40, 262 multichip module-L 248-249 wire bonding on 125-127 Plated deposits, metallurgical concerns, surface finishes 117 Polyimides 204 Polymer/bumps 161-163 conductive epoxy bumps 161-162 elastomeric bumps 162-163 Positive resist, comparison 25 Printed wiring board 250-251 wire bonding on 125-127 Printed wiring board assembly 34-35 Processes of manufacturing, overview 15 - 17

Q

Quad flat pack 35-36

R

Reliable wire bonding 112–115 Resistivity 203 aluminum 203

S

Screen printer 223–227 Screen printing 227–229 Semiconductor assembly/packaging/test process 81–83 Semiconductors 10–14 input/output, impact on package 13-14 input/output count, impact at chip level 12 - 13Sequential laminar circuitry 263 IBM 253-256 level 2.0 high density interconnect printed wiring board 255-256 Silicon dioxide 204 Silicon wafer 16 Silver, resistivity 203 Single chip packaging 31–45 area array packages 36-41 ceramic ball grid array 38 plastic ball grid array 38-40 tape ball grid array 40 ball grid array 36-41 attributes 42 concerns 42-43 surface mount assembly 41-42 evolution, integrated circuit packaging 32 - 33flat pack 34–35 future 43 input/output count 32-33 integrated circuit package 31-44 lead-free manufacturing 43–44 processing 44 pin grid array, ball grid array 36-41 printed wiring board assembly 34-35 quad flat pack 35-36 surface mount technology 34-35 trends 32-36 Single chip pin count 11 Singulated die chip scale package 48-49 Soft substrates, organic substrates, wire bonding on 126-127 Solder bump materials, reflow temperatures for 147 Solder joint reliability, flip chip 173–182 corrosion 181-182 electromigration 181 flip chip encapsulation/underfill 177-178 intermetallic compounds 181 materials properties, organic substrates 176 silicon cratering 182 solder fatigue 174-180 underfill processes 178-180 Solder reflow attach 183 Solder reflow process 170–173 Stacked packages 68 Stud/ball bumping 163-165

Substrate/package technologies 62 Subtractive etching vs. selective plate-up process 201-211 conductor materials 202-203 dielectric materials 203-205 semi-additive process 201 silicon substrate 210-211 substrates 207-210 subtractive etch process 201–202 thin film materials 202 via patterning in dielectric layers 206 - 207Surface mount technology 34–35 System in package/system on package 77-79 System on package vs. system on chip 78

Т

Tape automated bonding 129–140 applications 139 assembly 134-135 attachment to package/substrate 136 - 138automation 135-136 inner lead attachment processes 135 mounting 135-136 comparing tape options 133 key elements of 130 manufacture 131-133 Minimod 129 tape automated bonding tape 129-133 types 131–133 Tape ball grid array 40 structures 40-41 Technology drivers 3–7 levels of interconnect/packaging 4-7 manufacturing process 3-4 packaging options 4 Thermocompression bonding, advantages/ disadvantages of 109 Thermosonic bonding, advantages/ disadvantages of 110 Thick film technology 221–232 advanced thick film patterning processes 229-232 diffusion patterning process 229-230 photosensitive/photodefinable thick film patterning 230-232 multichip module-C/high density interconnect 227-229 pastes/inks 223 process 221-222 screen, screen printer 223-227

screen printing 227–229 Thin film process capability 194 Thin film technology 193–219 alternative thin film processes, multichip packaging applications 212-218 bumpless build up layer interconnect package 215-216 GE high density interconnect process 212-214 low cost "chips first" multichip module 214-215 benzocyclobutane 204 conductor metals 203 copper, resistivity 203 cost 218-219 dry film photoresist properties 197 electrodeposited photoresist properties 199 epoxies 204 fluoropolymers 204 gold, resistivity 203 high density interconnect substrate interconnect 200-201 high density package/substrate manufacturing technologies 193-219 inorganic materials, thermal properties 208 liquid crystal polymers 204 liquid resist, properties of spin on 197 mask aligner vs. 1X stepper 200 polvimides 204 resistivity 203 aluminum 203 silicon dioxide 204 silver, resistivity 203 subtractive etching vs. selective plate-up process 201-202 conductor materials 202-203 dielectric materials 203-205 semi-additive process 201 silicon substrate 210-211 substrates 207-210 subtractive etch process 201–202 thin film materials 202 via patterning in dielectric layers 206-207 thin film process capability 194 thin film technology 193-195 exposure systems 199–200 patterning process 195-200 photomask 196 photoresist 196-199, 201, 212, 220

yield 28, 218–219 Three-dimensional packaging 61, 67–71, 73 Three-dimensional plus technology 73 Transistor 1–14 Trends 32–36 Types of bonds 110 Types of multichip modules 65–66 Types of photomasks 22–23

U

Ultrasonic bonding, advantages/ disadvantages of 109 US FED STD 209E cleanroom standards 18

V

Verifying wire bonding quality 118–120 Vertical interconnect processes 75–77 Vias, high density interconnect 251–253 microvias 252–253

W

Wafer bumping 147–150 under bump metallization 148 deposition processes 148-150 bump metallurgy, selection 147-148 chemical deposition, electroless Ni/immersion Au process 149-150 deposition by evaporation, sputtering 149 Wafer bumping processes, comparing 161 Wafer level burn-in, test 90 Wafer level packaging 55–57 flip chip in package, vs. chip on board 100 processes 55-57 Wafer lot acceptance testing 86 Wedge bonding 111 Wire bondable organic substrates, insuring 126 Wire bonding 49–50