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A Random Trimming Approach for Obtaining High-Precision Embedded Resistors

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***Abstract* – Embedded resistors will potentially allow electronic applications to cost less and perform better. However, it is difficult to fabricate embedded resistors to the correct resistance value, so embedded resistors are often fabricated with a lower value and then trimmed to raise the resistance to the desired value. A computer simulation for the trimming process of an embedded resistor has been developed that has been verified and calibrated against experimental results. A study of embedded resistors containing random voids of varying size has been performed. A new trimming strategy in which the trims are made randomly (rather than conventional L-shaped trims) is proposed and the results of the analysis demonstrate that single-dive trimming combined with random trimming allows higher precision embedded resistors to be obtained than conventional trimming patterns.**

***Index Terms* – Embedded resistors, embedded passives, trimming, numerical simulation, random trimming, voids**

I. INTRODUCTION

The world demands a continuous stream of smaller, better performing, and less expensive electronic systems, such as cellular phones. One technology that enables these systems to become smaller and better performing is called embedded passives. Embedded passives are electrical components (most commonly resistors and capacitors) that are fabricated inside or on the surface of printed circuit boards instead of being mounted on them (we will refer to surface mounted passive components as "discrete" components).

Embedded resistors are fabricated in one of two ways: 1) subtractive processes – a layer with resistive material plated on it is etched to form specific resistors and then included within the printed circuit board layers, e.g., [1,2]; or 2) additive processes – resistive material is printed or plated onto a layer with other printed circuit board features to form specific resistors, e.g., [3].

However, embedded resistors have several problems that are preventing their widespread adoption. Processes for making resistor geometries are inexact requiring the resistors to be "trimmed" if high precision is required. Resistors are normally fabricated to lower resistance values than needed and trimmed by cutting holes in them with lasers to increase their resistance value [4]. There are several desirable trimming characteristics: precision (getting as close to the target resistance as possible); minimizing the risk of trimming too much (if a resistor is "over-trimmed," it is usually not practical to fix it and the board will have to be thrown away); and minimizing the length of each trim (a longer trim takes more time to make and impacts throughput thereby costing more money). Voids in the resistive material complicate the trimming problem, especially for high-precision resistors; if a void is encountered during trimming, the resistance may "jump" uncontrollably to a higher value beyond the target resistance. Although the density and size of voids is a function of the process and materials used to create the embedded resistors, nearly all types of embedded resistors have reported some amount of voiding, e.g., polymer thick-film resistors [5,6], thin-film resistors [7].

Various trimming patterns are used today to meet the desired trimming characteristics. Common practice is to use "L" shaped trims ("L-cut") (see Fig. 1), where a cut perpendicular to the current flow in the resistor quickly increases the resistance to near the target value, then a change in direction of the trim to parallel to the current flow

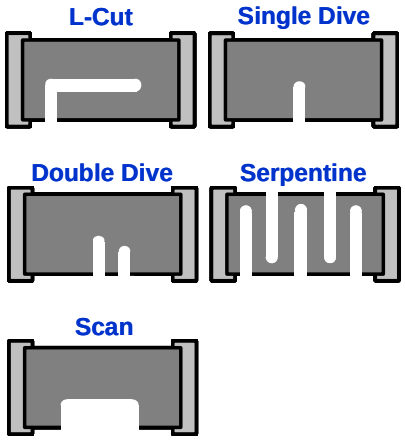

Fig. 1. Various resistor trimming patterns.

slows down the change in resistance to reach the target. Other common trimming patterns include "single-dives": trimming straight into the material; "double-dives": trimming straight into the material in two locations; "serpentine" trims; as well as several other patterns and variations thereof, [4].

This paper describes a numerical simulation model verified experimentally by trimming resistive paper. The model is used to compare the efficiency of L-Cut trimming patterns and a new random trimming pattern applicable to high-precision embedded resistors. The experimental trimming approach is described in Section II, and Section III provides the formulation of the simulation model. In Section IV, L-cut trimming and the new random trimming approach are assessed and compared based on number of trimming steps required and the precision of the resulting trim.

II. Experimental Analysis

To emulate embedded resistors experimentally, trimming of resistive paper has been performed, [8]. For a constant sheet resistance (ohms per square), the resistance of a planar resistor does not change with size (i.e., length or width) as long as the ratio of length to width (aspect ratio) is constant,

$$R = \frac{\rho L}{A} = \frac{\rho L}{TW} = \frac{\rho}{T}\left(\frac{L}{W}\right) = R_{\square}\left(\frac{L}{W}\right) \tag{1}$$

where ρ is the bulk resistivity, A is the cross-sectional area of the resistor, $R_{\square}$ is the "sheet resistance" (in ohms per square), and L, W, and T are the length, width, and thickness of the resistor. Therefore, a small planar resistor (dimensions in the thousandths of the inch) has the same resistance characteristics as a large area planar resistor (dimensions of inches), and trimming of small resistors can be emulated using larger area resistors.

Multiple sheets of resistive paper (PASCO Scientific, Model Number PK-9025) were cut into 28x10 centimeter sheets. Silver contacts were added to the two ends of each resistor using silver conductive paint. Metal clamps were used to connect to the resistor contacts and ohmmeter probes were then connected to the metal clamps. The silver contacts were found to make the resistance measurements less sensitive to the placement or pressure applied by the clamps.

The resistance of the resistive paper was found to vary from sheet to sheet (probably due to thickness variations in the resistive material used to coat the sheets). In order to make measurements from multiple sheets comparable, the measurements were normalized. The "normalization" process scaled all measurements from each sheet to 65 kΩ.[1] To normalize the various sheets to 65 kΩ, 10-15 initial measurements from each sheet were made prior to trimming, the measurements were averaged, and the average was divided by 65 kΩ to obtain a scaling factor that was specific to the sheet. Every measurement taken from the specific sheet thereafter (during trimming) was multiplied by this scaling factor before comparison with data from other sheets. The normalization process was performed for every resistor used in the experimental study. This normalization procedure accounts for variations in the sheet resistance from sheet-to-sheet only (variations in series resistance in the measurement path are not affected, e.g., clamp pressure). Series resistance variations are reflected in the standard deviation in the measured resistance after normalization, which was found to be 0.9% (0.59 kΩ) from over 500 measurements.

III. Numerical Simulation of Resistor Trimming

A numerical simulation of embedded resistors that allows variation in trimming patterns was implemented, calibrated, and verified using the experimental results from trimming resistive paper. Previously reported numerical simulations of trimmed embedded resistors include: models for predicting the performance of laser-trimmed resistors taking into account the heat-affected zone around the trim [9,10]; numerical trim simulations that were demonstrated in the resistor design process to predict trimmed resistor results [11-13]; and three-dimensional simulators that have been utilized in calculations of interconnect structures, [14]. Non-simulation mathematical models have also been developed for several specific trim patterns, [8]. The model used in this work is a finite difference model formulated similarly to [9] and is summarized in the following paragraphs.

[1] 65 kΩ was chosen as the normalization target because it was the mean resistance of the untrimmed 28x10 cm sheets of resistive paper, see [8].

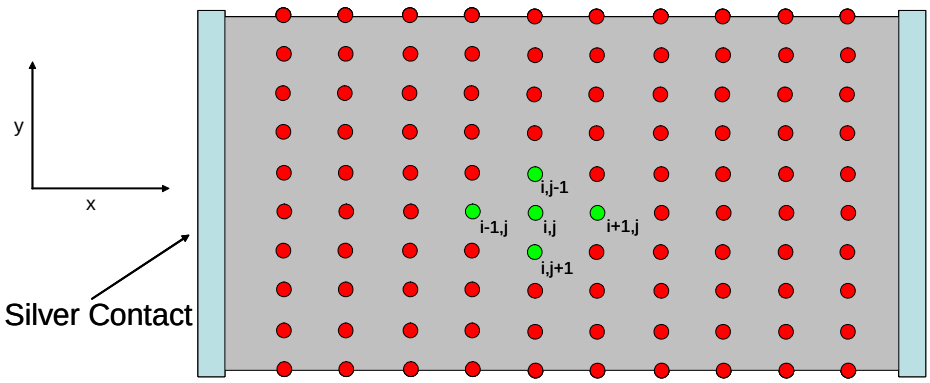

Fig. 2. Example 10 x 10 grid superimposed on a resistor with grid points (i, j).

A. Model Formulation

A grid is superimposed on the resistor as shown in Fig. 2. We assume that the resistor is uniform in the third dimension (into the board), so we are interested only in the two-dimensional problem. To determine the resistance of the embedded resistor, the voltage at each of the grid points must first be determined. The voltage is found by solving Laplace's Equation in two dimensions at each grid point,

$$\nabla^2 V = \frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = 0 \tag{2}$$

where V is the voltage. Assuming that the distance between the grid points in the x and y directions are the same, a finite difference technique was used to expand Laplace's Equation as,

$$V_{i,j-1} + V_{i-1,j} - 4V_{i,j} + V_{i+1,j} + V_{i,j+1} = 0 \tag{3}$$

For the 10 x 10 grid shown in Fig. 2, we write an equation like the one above for every grid point. The system of equations is solved by writing the set of equations in the form of a matrix equation:

$$[\ ][\ ] = [\ ]$$

System of equations — Voltages at every point (unknowns) — Constant Matrix

A Gaussian Elimination technique is then used solve the matrix equation for the voltages at every point.

Once the voltages at all the points have been solved for, the electric field ($\overline{E} = -\nabla V$) at every point can be found, and the current density at every point is given by,

$$\overline{J} = \sigma\overline{E} = \frac{\overline{E}}{R_{\square}} \tag{4}$$

where σ is the conductivity and $R_{\square}$ is the resistivity (Ω/□) of the material. Using Ohm's Law, the resistance can be found,

$$R = \frac{V_{applied}}{\sum_{\gamma} J_x \Delta y} \tag{5}$$

where γ is any line connecting the top and bottom (non-contact edges) of the resistor and Δy is the grid spacing in the y direction.

B. Boundary Conditions

On the contact ends of the resistor, the voltage is known (Dirichlet boundary condition). On the top and bottom of the resistor, the electric field perpendicular to the boundary must be zero (Neumann boundary condition),

$$\overline{E} = -\nabla V = -\frac{\partial V}{\partial x}\hat{x} - \frac{\partial V}{\partial y}\hat{y} \tag{6}$$

so, at the top and bottom boundary,

$$E_y = -\frac{\partial V}{\partial y} = 0 \tag{7}$$

Trims into the resistor and voids in the resistive material require setting a Neumann boundary condition on the edges of the trim or the void.

C. Experimental Verification and Calibration

The simulator was verified against experimental results using resistive paper by both probing the voltage in the resistor and measuring the resistance as a function of trimming the resistor as shown in Fig. 3.

We also had to calibrate the trim spot size in the simulator. This was performed by experimentally trimming one spot successively larger in an experimental resistor sheet until the resulting resistance matched the resistance on a 1 x 1 grid cell trimmed in the

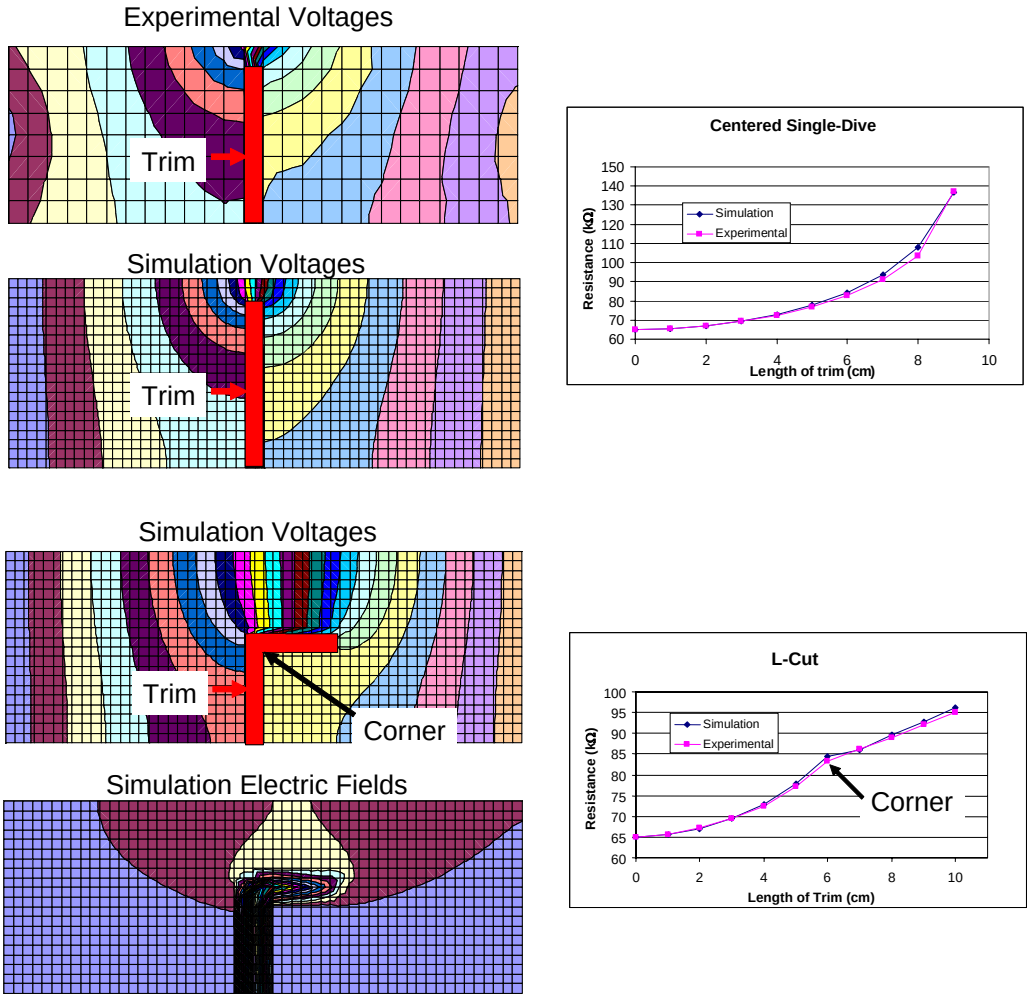

Fig. 3. Simulation verification for a single-dive and an L-cut trim using comparison with experimental results.

simulator. This calibration was extremely important in order to assess randomly trimmed resistors (see Section IV).

IV. Trimming Analysis

Trimming must be able to reach a target resistance precisely for embedded resistors that may contain voids. If a void is encountered during trimming, the resistance can jump beyond the target value. Precision measures how close to the target resistance the trim can get. A methodology that utilizes random (unpatterned) trimming was found to

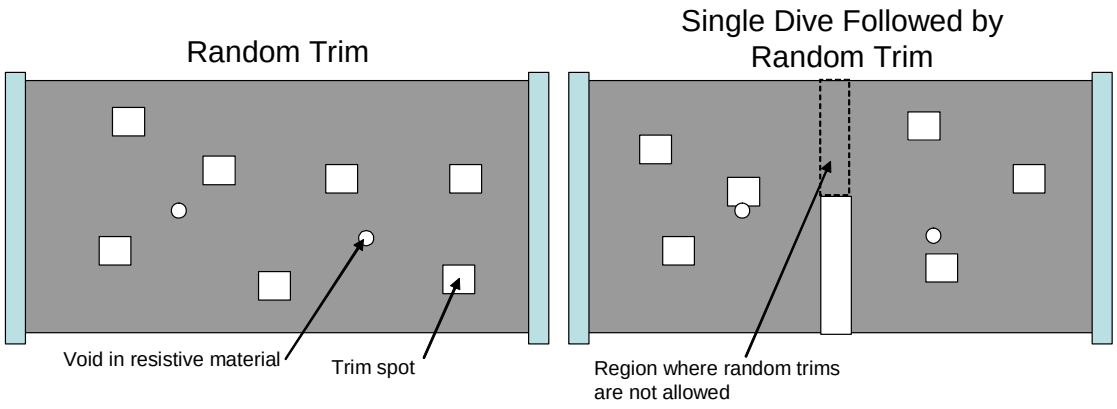

Fig. 4. Random trimming. Left – pure random trimming; right – single-dive first then random trim to target. Example voids are also indicated.

increase resistance in embedded resistors more controllably than L-cuts, thus potentially allowing higher precision resistors to be obtained even when voids are present in the material. The "random" trimming technique introduced in this paper has unique properties that cannot be easily obtained using other trimming patterns.

Random trimming is performed by choosing a point on the resistor at random, and then "firing" a hole into that position as shown in Fig. 4. Random trimming by itself (left side of Fig. 4), although well controlled, is generally too long of a process, i.e., takes too much time because too many holes have to be made. So, random trimming was combined with the single-dive trim in the following way: a single-dive was performed to reach to a target resistance range quickly, and then the random trim was implemented to get as close to the target resistance as possible. If a random trim happens to coincide with or touch a void, the effect on the resistance is intuitively much less than it would be if a void was encountered on the edge of one of the fixed trimming patterns shown in Fig. 1. We also found it necessary to define the current channel region between the end of the single-dive and the edge of the resistor as an area where random trims were not allowed in order to better control the resistance change.

Note, the random trimming approach suggested herein differs from the "swiss cheese" approach suggested in [10], where a set of trim targets are initially created as holes in the resistor and then cuts from the edge of the resistor to the targets are performed. In our approach, after an initial single-dive trim into the resistor, random trims are made. This approach decreases the heat-affected portion of the resistor (as does

the approach in [10]),[2] and provides a controlled approach to the target resistance that minimizes the sensitivity of the trim to voids that may be present in the resistor material. The following section quantifies the performance of random trimming relative to L-cuts.

A. Analysis Strategy

The following steps were performed to obtain qualitative and quantitative results from the numerical simulation: for a resistor with a specific number of randomly placed voids of a specific size: 1) randomly place the voids in the resistor, 2) perform a single-dive to a specific depth (specified percentage of target resistance), and 3) perform either an L-cut (conventional approach) or random trim (proposed new approach) to reach the target resistance. Steps 2 and 3 are then repeated from a series of random void placements. The whole process was repeated for a range of void densities (number of voids per resistor) and void sizes.

B. Results

For the example shown in Fig. 5, the target resistance is 100 kΩ.[3] When trimming with a single-dive, the resistance increase per trim step near the target is 3.8 times greater than that of an L-cut, and 15 times greater than that of a random trim. This result demonstrates that the random trim results in a significant increase in precision compared to the single-dive and L-cut. The closer trimming can get to the target, the more precise a resistor can be fabricated. Higher precision trimming allows a larger fraction of the resistors in a system to be embedded (as opposed to discrete).

The result in Fig. 5 is an example for a single resistor without voids. To statistically demonstrate random trimming's precision advantages, trimming was performed on resistors with a range of void densities (1-6 voids per resistor) and void sizes in the 28x10 centimeter resistors (4 different void diameters: 1.0 centimeter, 1.5 centimeters, 2.0 centimeters, and 2.5 centimeters).

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[2] The heat-affected zone is the area of untrimmed resistive material adjacent to the trim that is effected by the trimming process, i.e., its physical properties change (sheet resistance, thermal conductivity, temperature coefficient of resistance), [9].

[3] All the results in this section are for resistor sizes that correlate to the resistive paper experimental results. However, the results in this paper should be generally applicable to different size resistors.

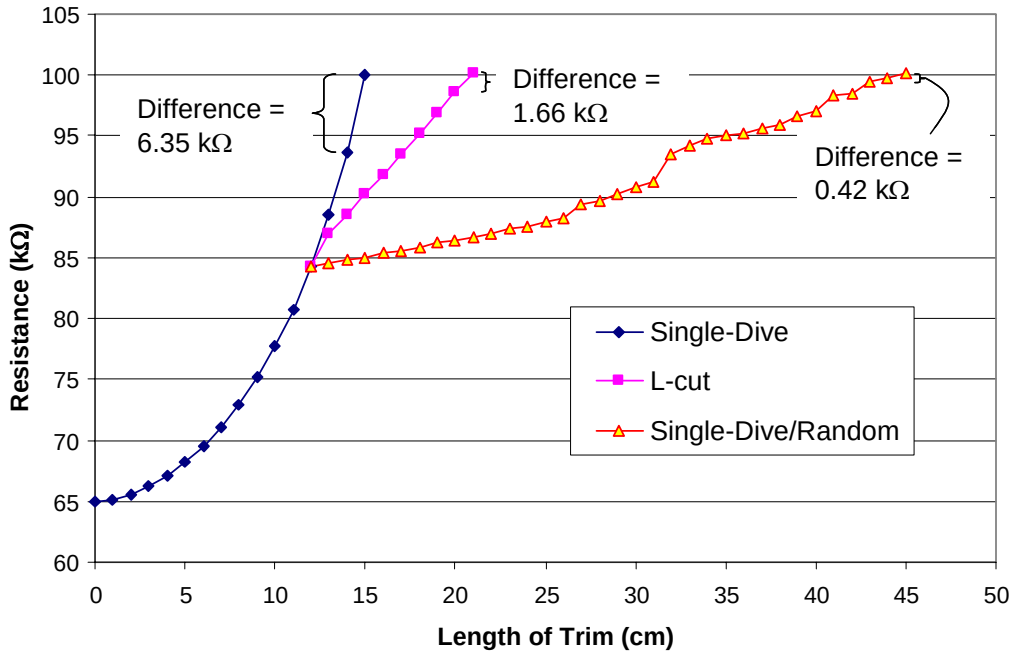

Fig. 5. Random trimming allows a significant increase in precision compared to the single-dive and L-cut. (Resistor dimensions: 28 cm x 10 cm, resistive paper)

Analyses were performed by varying the stopping criterion for the single-dive. Fig. 6 shows an analysis for initial single-dive depths ranging from 82.5% of the target to 94% of the target. If the single-dive is allowed to go as far as possible without over-trimming (which can be done with the simulation, but would be impractical for real resistors; not shown on Fig. 6) random trimming reduces the mean error after trimming from 1.8% for L-cuts to 0.46%.

The result in Fig. 6 shows that the precision obtained from L-cuts decreases as the initial single-dive goes further into the resistor; however, the precision that can be obtained from the random trim is approximately independent of the length of the initial single-dive.

The result in Fig. 7 shows that the number of trimming steps necessary to reach the target decreases as the initial dive depth increases and is always larger with random trimming (as would be expected). However, the result in Fig. 6 suggests that the single-dive/random trimming combination can be practically used with an initial dive depth of 93.4% or larger (the precision appears to be unaffected up to at least 93.4%), while L-cuts

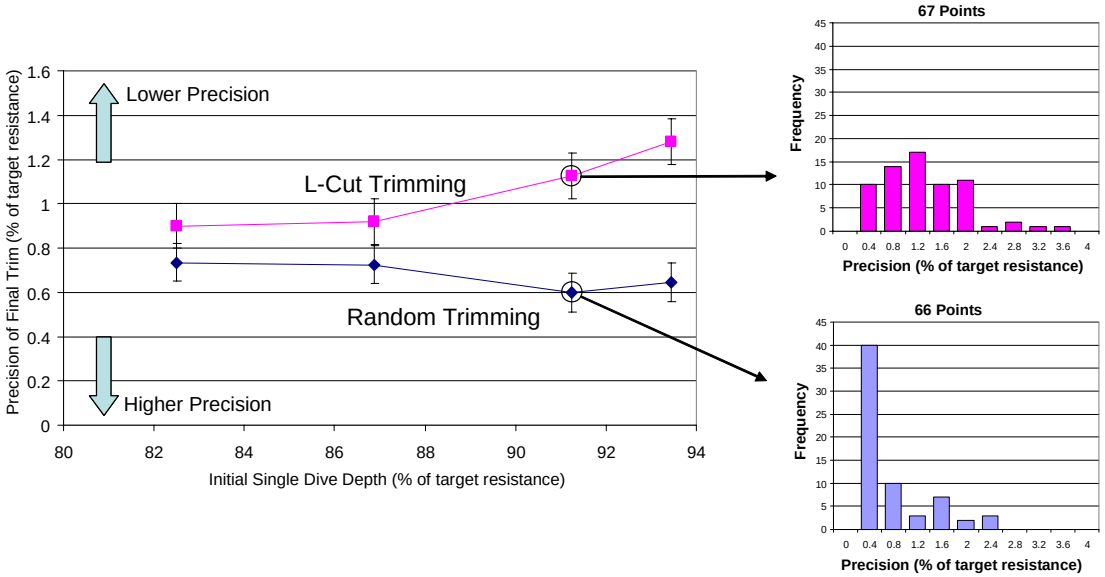

Fig. 6. Trimming precision as a function of stopping criteria. Each data point represents the mean of 55 or more void density/void size combinations.

are probably practically limited to an initial dive depth of 87% or less. Table I compares the highest precision L-cuts with the most efficient random trims. Table I indicates that a 29% increase in precision can be obtained for a 17% increase in the number of trim steps. This result suggests that random trimming should not be used for all embedded resistors, rather only used for those that require precision levels that cannot be attained using L-cuts.

TABLE I
COMPARING THE HIGHEST PRECISION L-CUT TO THE MOST EFFICIENT SINGLE-DIVE/RANDOM TRIM

	Initial single-dive depth as % of target (Fig. 6)	Number of trimming steps to target (Fig. 7)	Precision as % deviation from target (Fig. 6)
Highest Precision L-cut	87%	20	0.92%
		Δ=17%	Δ=29%
Most efficient single-dive/random trim	93.4%	24	0.65%

V. SUMMARY AND CONCLUSIONS

A study of embedded resistors with random voids of varying size was performed. A new trimming strategy in which the trims are made randomly (rather than conventional

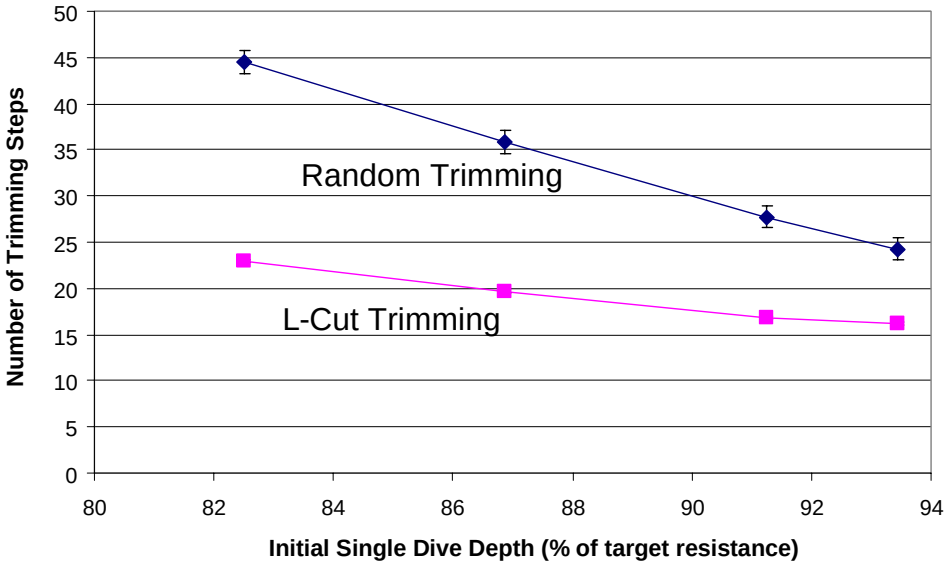

Fig. 7. The number of trim steps necessary to reach the target resistance. Each trim step is an equal cut distance (in the case of the resistive paper, this is 1 cm), so the number of trim steps is proportional to the total length of the trim. Each data point represents the mean of 55 or more void density/void size combinations.

L-shaped trims) has been proposed and the results of the analysis demonstrate that single-dive trimming combined with random trimming allows higher precision embedded resistors to be obtained than conventional trimming patterns. Results suggest that the single-dive/random trimming combination is both a practical way to trim embedded resistors containing voids and a potentially better way to trim *all* embedded resistors when high precision is required.

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